DEVELOPMENT OF A SOLID-STATE FAULT CURRENT LIMITING AND INTERRUPTING DEVICE SUITABLE FOR POWER DISTRIBUTION NETWORKS

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BSc MSc AMIEE MIEEE

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Dedication

To

My Parents, My Wife

My Sisters, My Brother RAMADAN

and My Kids

MOSTAFA, EMAN and AHMED

UNIVERSITY OF NORTHUMBRIA AT NEWCASTLE

Thesis Declaration

TITLE OF THESIS	**DEVELOPMENT OF A SOLID-STATE FAULT CURRENT LIMITING AND INTERRUPTING DEVICE SUITABLE FOR POWER DISTRIBUTION NETWORKS**
AUTHOR	**MOHAMED MOSTAFA RAMADAN AHMED**
IN COLLABORATION WITH	**Northern Electric Distribution Limited**

Signed _____

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All my thanks to ALLAH

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Abstract

In recent years there has been an increased interest in developing fault current limiters for power distribution networks. This arises from the need to cope with the ever increasing short-circuit levels and to reduce the stress on system equipment, e.g. transformers, circuit-breakers and cables. It is also due to the increased concern about power quality, where fault current limiters are expected to play an important role in mitigating voltage sags during faults. Various devices to limit the fault current have been proposed, such as controlled fuses, tuned LC circuits, solid-state and superconducting fault current limiters.

This research investigate the use of a novel technique to develop a solid-state Fault Current Limiting and Interrupting device (FCLID) suitable for low voltage distribution networks. The FCLID mainly consists of a high-speed bi-directional semiconductor switch, a varistor (non-linear resistor) and a snubber circuit; all connected in parallel. The semiconductor switch and the varistor share the fault current during the period of FCLID operation.

To protect the semiconductor switch and the varistor from damage due to overheating, their temperatures are indirectly monitored in order to define the maximum operating time of the FCLID. A new method for estimating the junction temperature of the switching device and the varistor under transient condition has been developed and experimental tests were carried out to validate the proposed method. The energy handling capability of varistors and associated problems due to their non-linear characteristics have also been investigated. Experimental tests were carried out to measure the energy

handling capability of the varistor using thermal imaging system. A new method for improving the current sharing between parallel varistors has been implemented.

A computer model of the FCLID has been developed and implemented into a typical distribution network using MATLAB/ SIMULINK. The network performance under different conditions has been analysed. An experimental single-phase 230 V prototype FCLID was developed and tested under different operating conditions.

Finally, the outcome of the theoretical, simulation and experimental phases of the research was used to establish the outline design specifications of a FCLID suitable for 11 kV distribution networks.

Contents

Glossary of Abbreviation

ABM	Analogue Behaviour Modelling
ASVC	Advanced Static Var Compensator
ATP	Alternative Transient Program
BEI	Back-Scatter Electron Image
D-STATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
EMTDC	Electromagnetic Transient for DC
EMTP	Electromagnetic Transient Program
ETO	Emitter Turn Off Thyristor
FCID	Fault Current Interrupting Device
FCL	Fault Current Limiter
FCLD	Fault Current Limiting Device
FCLID	Fault Current Limiting and Interrupting Device
FFT	Fast Fourier Transform
GTO	Gate Turn Off Thyristor
HFCLID	Hybrid Fault Current Limiter
IGBT	Insulated Gate Bipolar Transistors
IGCT	Integrated Gated Commutated Thyristor
MCT	MOSFET Controlled Thyristor
MOV	Metal Oxide Varistors
NEDL	Northern Electric Distribution Limited
PC	Personal Computer
PCC	Point of Common Coupling
R.M.S.	Root Mean Square value
SAM	Scanning Acoustic Microscope
SCFCL	Supperconducting Fault Current Limiter
SEI	Second Electron Image
SEM	Scanning Electron Microscope

SMPS	Switched Mode Power Supply
SNT	Sequential Network Tripping
SSCB	Solid State Circuit Breaker
SSFCL	Solid State Fault Current Limiter
STSSS	Static Transfer Solid State Switch
TCSC	Thyristor Controlled Series Capacitor
VCB	Vacuum Circuit Breaker
ZnO	Zinc Oxide

CHAPTER ONE

INTRODUCTION

1.1 Fault Current Level

Existence of high fault currents in a power system is an old problem and several solutions have been proposed based on different principles [1-12]. The fast growth of electric-energy demand resulted in a corresponding increase in short-circuit currents. Consequently, fault current limiters (FCL) were used to reduce the line breaker rated capacity and to limit the electrodynamics stress. The main problems to solve were the FCL reliability, which has to be as high as possible, and the speed of the intervention, which must be high enough to limit the first peak of the fault current. In addition, a FCL device can also be regarded as an effective mean to compensate for the short-circuit related voltage sags in distribution utilities. Therefore, a FCL devices can be used to improve the quality of the power supply. Based on the literature review of old and new fault current limiters, there is no device that can fulfil all the requirements of modern power systems. For this reason, this research investigates the operation of a new device.

THIS CHAPTER presents an overview of available fault current limiting and interrupting devices for protecting power distribution networks. Some of these devices were installed in distribution networks for long periods while other are still in the development stage. Attention is focused on solid-state fault current limiting and interrupting devices, which are the subject of this study. Finally, the objectives of the research reported in this thesis are discussed and original contributions are outlined.

1.2 Possible Solutions to Limit The Fault Current

A fault on a power system is a localised failure of the electrical insulation which results in a heavy current to flow to earth or between live conductors. Failure might arise from overvoltages such as lightning striking an overhead line, mechanical damage by an external agent, ageing or thermal degradation of the insulation material. The flow of fault current may cause further damage by heat from the arc at the fault point, by ohmic heating by the current in other parts of systems, and by magneto-mechanical forces especially on transformer windings. There is also a dip in the voltage at the terminals of a plant connected to the line; such a dip in voltage might prevent this plant from performing its normal duty and lead to damage of equipment.

Possible solutions to combat the increased fault level are [13]:

- Splitting the grid and providing interconnections through higher voltage a.c. or d.c. link i.e. splitting the system into a number of islands.
- Splitting of buses and sequential network tripping (SNT).
- Replacing the existing equipment with others of higher rating.
- Implementing fault current limiters.

The first two are operational methods in which electrical separation of a power system is required where the benefits of system integration are lost and eventually duplication of system facilities would be required. Momentary fault currents are not reduced in sequential tripping. The third option can be very expensive and also during the long replacement period, reliability and availability of the system are impaired.

The most modern ultra-fast circuit-breakers operate in about one cycle. Though such a breaker can protect the installation against thermal effects, it can not fully avoid the

effects of the dynamic forces (proportional to the square of the current). A revision of power system protection calls for a device that is able to prevent the fault current from reaching its prospective value well before the peak first half cycle. The introduction of FCLs in a system is an economic way of accommodating higher fault levels without compromising system performance.

The primary operational benefit of a fault current limiter would be the reduction of current stresses on power system equipment during a fault [14]. The economic benefits include:

- Increased substation transformer life by reducing the let-through current.
- Elimination, or at least minimising, conductor damage and burndown.
- Elimination of special current limiting fuses on high voltage circuits.
- Increased substation transformer capacity by allowing parallel operation of transformers during normal and contingency periods.
- Improved customer relations by reducing voltage sags on non faulted circuit fed from the same source as the faulted circuit.

1.3 System Requirement for Fault Current Limiters

The commercial success of a fault current limiter at distribution or transmission levels depend on how cost effective it is as compared with highly competitive one [15]. Ideally, fault current limiters are required to have the following performance characteristics:

- Low or zero impedance under normal operation.
- High impedance under fault conditions.
- Fast transition from normal to limiting state.
- Fast recovery to normal state after fault interruption.

- Insensitive to normal overload currents, including transformer energising, discharging of capacitor banks and motor starting.
- High dielectric strength to transient overvoltage during fault condition.
- No adverse effect on the selectivity of the protection system.
- High reliability with minimum maintenance.
- Compact size.
- Low cost.
- Light weight.
- Fail safe operation.

Fault current limiters can be installed at locations where short circuit levels exceed rating of the power system components. Fault current limiter can be used at transmission or distribution voltage levels, at bus ties, incoming feeders, outgoing feeders and generators feeders locations. Connected in series with the system, the fault current limiter has to carry the full load current all the time and therefore its normal resistance should be very small in order to minimise power losses i.e., to minimise cooling cost throughout the fault current limiter's working life.

1.4 Types of Fault Current Limiters (FCLs)

Fault Current Limiters can be divided into two main classes: one class comprises single-shot devices, such as current-limiting fuses which may also interrupt the fault current; the second class includes multi-operation devices such as superconducting, and semiconductor FCL. Many of the multi-operation devices commutate the fault current into a parallel impedance (resistive or inductive) which limit the let-through current.

Other multi-operation FCL utilises tuned circuits or non-linear elements that produce an increase of impedance at the sensing of a fault current.

1.4.1 Current limiting fuse

A fuse is often used for current limitation. Fault current limiting fuses are able to interrupt the fault current before the first peak. The need of replacement after every operation is a major drawback which make them incompatible with HV system. A Fuse operation may generate overvoltages.

1.4.2 Supperconducting fault current limiters (SCFCL)

The phenomenon of superconductivity is exhibited only when the magnetic field, current density and temperature are below some critical values (Hc, Jc, and Tc). Should any of these parameters be exceeded, the superconductor becomes 'normal' i.e. normal conductive resistance appears [16,17]. This is known as quenching. The fast and sharp transition from superconducting state to normal state is used to limit the fault current. One advantage of this is that there is no need to use devices for detecting the fault current and tripping the limiter.

Basically, two method are employed; the resistive method shown in Figure (1.1) uses a superconducting element for transferring the fault current to a shunt resistor thereby limiting it. Under normal condition, the current flows through the superconductor, when a fault occurs the resistance of the superconductor become greater than the shunt resistance which limit the short-circuit current. The limiter is disconnected from the circuit by a series connected circuit-breaker for a minimum duration to allow for a cooling-down

phase. It is only switched on again automatically when it reaches its superconducting state.

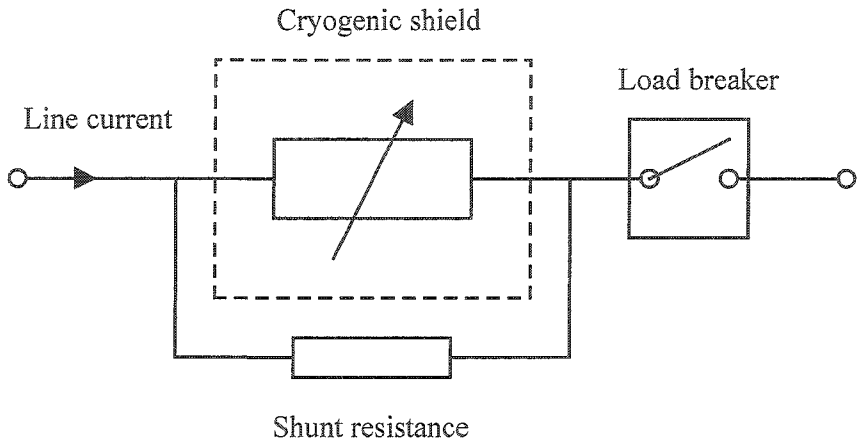


Figure 1.1 Resistive fault current limiter

The second method, known as inductive method, uses a system of coupled coils in which the secondary winding is connected to the superconducting material as shown in Figure (1.2). During normal operation, coupled coils consisting of a normal conducting primary coil and a secondary coil act as a short-circuited transformer, so that a low impedance is exhibited at the primary side. When a fault occurs, the current induced in the secondary coil becomes too high resulting in a change in the state of the Supperconducting material. A high impedance value will then appear on the primary side and it limits the fault current. The disadvantage of this principle is the fact that the magnetic field now present, leads to losses in the secondary circuit, which means that it is necessary to install a circuit breaker to interrupt the limited current. In contrast to the inductive SFCL, the resistive type require current leads (to prevent heat transfer form the normal conductor to the superconductor) but is nevertheless lighter in weight and require less space.

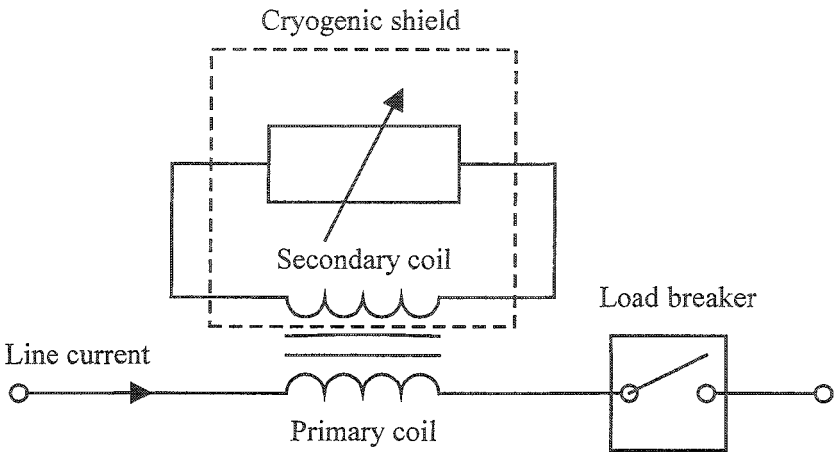


Figure 1.2 Inductive fault current limiter

The disadvantages of the Supperconducting FCL are as follows:

- It can not limit the fault current to a very low value (typically about one-third of the prospective fault current).
- Bulky.
- Need a circuit breaker to interrupt the current in case of permanent fault.
- Cooling cost is high.

1.4.3 Series-parallel resonant FCL

The series-parallel resonant, developed by Westinghouse [18], employs a series tuned inductor-capacitor circuit which is rapidly changed into a parallel tuned circuit to increase the circuit impedance. Figure (1.3) shows two parallel branches with a reactor and a capacitor in each of the branches. The bridging circuit consists of a resistor and a switch. This circuit arrangement is connected in series with the line where the fault current desired. During normal operation the switch 'S' is open. The two parallel branches represent series LC circuits, and each is tuned at 50 Hz, resulting in zero net impedance.

When a fault occurs, switch 'S' is closed, inserting a resistor R between the two LC circuits and limiting the fault current. The resultant impedance of the circuit is X^2 / R, where X is the 50 Hz impedance of the reactive components.

The disadvantage of this limiter:

- The impedance of this limiter is designed for one level and one type of fault.
- A circuit-breaker is required to interrupt current.
- Expensive and bulky (the components rating and size are directly proportional to the throughput MVA rating).

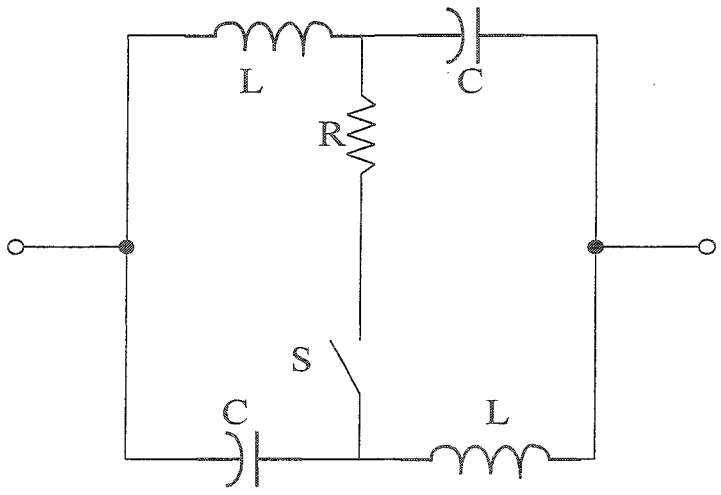


Figure 1.3 Series-parallel resonant FCL

Figure (1.4) shows the schematic principle for the series-parallel resonant FCL using thyristors instead of the mechanical switch [19]. Thus, there is a large flexibility in the selection of X & R to obtain the desired impedance. The disadvantage of this type of FCL is the rather high voltage across the thyristors (double that across the reactor or the capacitor). Such a voltage is line current proportional and rapidly increasing in case of the short-circuit. Also, a fast sensing element is essential.

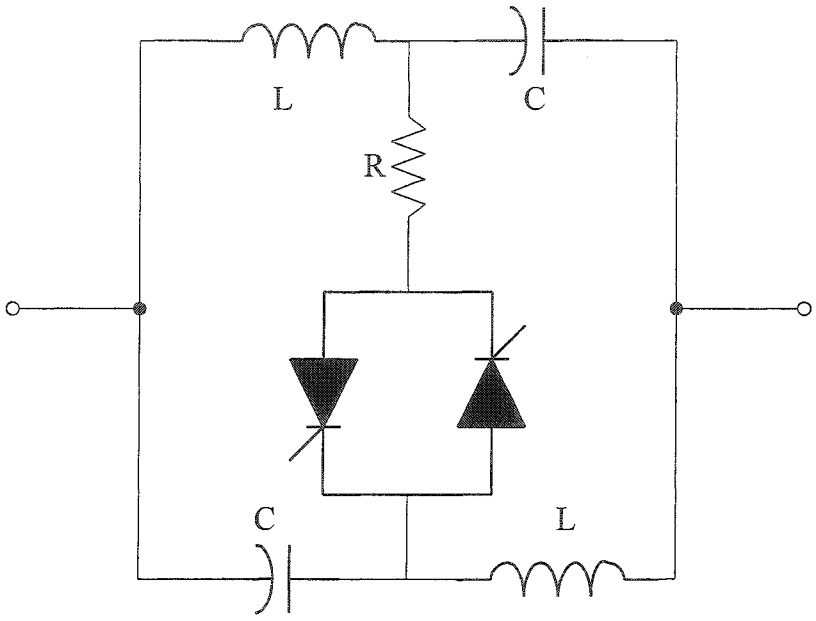


Figure 1.4 Series-parallel resonant FCL using thyristors

1.4.4 Resonance FCL

This device limits the fault current by inserting an impedance of a resonant LC circuit in series with the line. In the normal conditions, the resonant circuit impedance is very large, theoretically infinite, if the losses are neglected. In case of the fault occurs the resonant impedance has to be switched into the circuit immediately, this can be achieved by using thyristors or GTO thyristors.

This is useful when capacitance C is connected in series with the line to provide series compensation, as shown in Figure (1.5) [20]. When a short-circuit occurs, thyristors TH-1 and TH-2 are fired, which connects inductance L in parallel with the capacitor. The resulting resonant circuit limits the fault current. The time to switch into this mode is extremely low, in order of milliseconds. Following turn-on, the thyristor switches at current zero, until the current is reduced to levels which can be mechanically interrupted.

Removing the gate firing turns off the thyristors switch at the next zero crossing, which restores normal operation if the fault is eliminated.

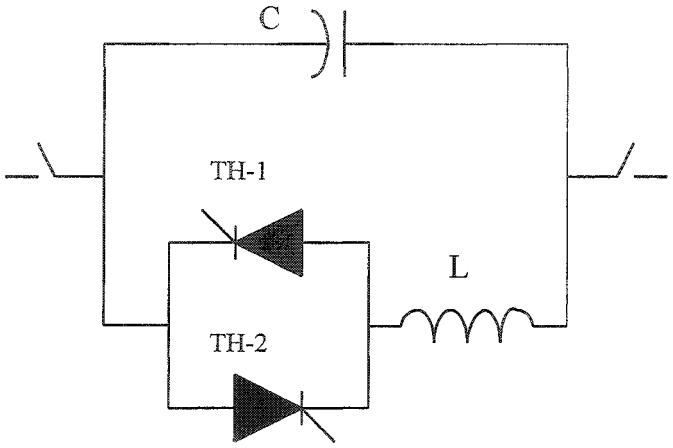


Figure 1.5 Basic arrangement for a resonant FCL using thyristor

Figure (1.6) utilises GTO thyristor switches, which are on during normal operating conditions [20].

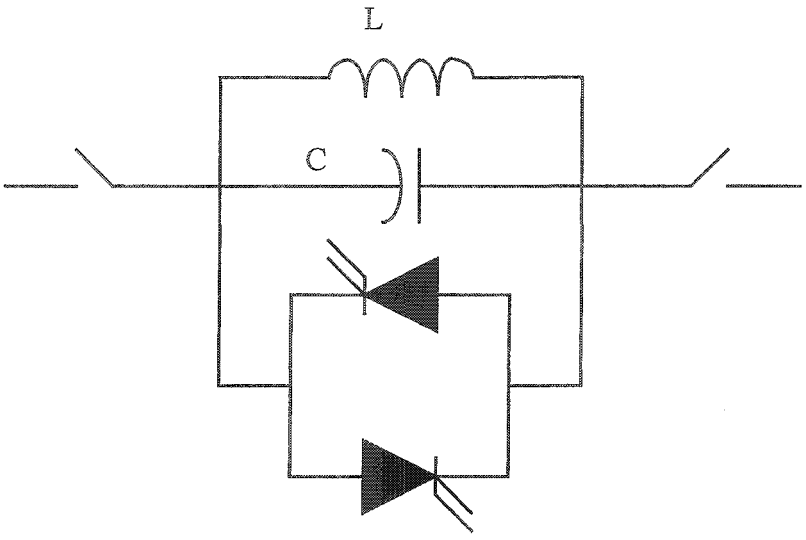


Figure 1.6 Basic arrangement for a resonant FCL using GTO

When a fault occurs, the GTO switches are turned off, and the current is diverted into the resonant circuit, which limit the fault current. Comparison of this circuit with that shown in Figure (1.5) shows that the thyristors in Figure (1.5) are conducting only during the

fault. Capacitance C, which is connected in series with the line in normal operation, compensates the line voltage drop. The GTOs in Figure (1.6) carry the load current continuously, which generates losses during normal operation and requires larger, more expensive switches. The formation of the resonant circuit in Figure (1.5), when all the switches are on, is a fail-safe design, because the most probable failure mode of the thyristor switches is the short-circuit.

1.4.5 Solid-state fault current limiter

Figure (1.7) shows a block diagram of the solid-state current limiter developed by Ueda in 1993 [21]. It consists of a fast solid-state switch, a current limiting impedance, a voltage limiting element, a series circuit-breaker, an overcurrent detector and a control device. The current limiting impedance is connected in parallel with the solid-state switch so that the current continue to flow, but at a limited level, after the solid-sate switch interrupts the fault current. GTO thyristors have been used as they can interrupt the current instantly upon receiving a turn off signal. The sudden interruption of current tends to cause an overvoltage which in this case presented by the parallel impedance. The series circuit-breaker switch is used for load switching and isolation. The overcurrent detector and control device detects the fault and produce turn-off and turn-on signals for the GTO thyristor. When a fault occurs, the over-current detector initiate a turn-off signal to the solid-state switch which interrupt the current immediately, e.g. within 1 ms. The short-circuit current is commutated to the current limiting impedance. If the fault is cleared by down stream protection devices, current continue to flow to other consumers through the FCL impedance and the solid-state switch is switched on again. For a feeder fault near the FCL, the fault current continues to flow and the series circuit-breaker is immediately

activated to isolate the fault.

The disadvantages of this scheme are as follows:

- Continuous conduction losses.
- Cooling cost.
- Lack of co-ordination due to the limited operating time (due to higher losses in the limiting impedance).
- Need for a series circuit-breaker to interrupt the fault current.

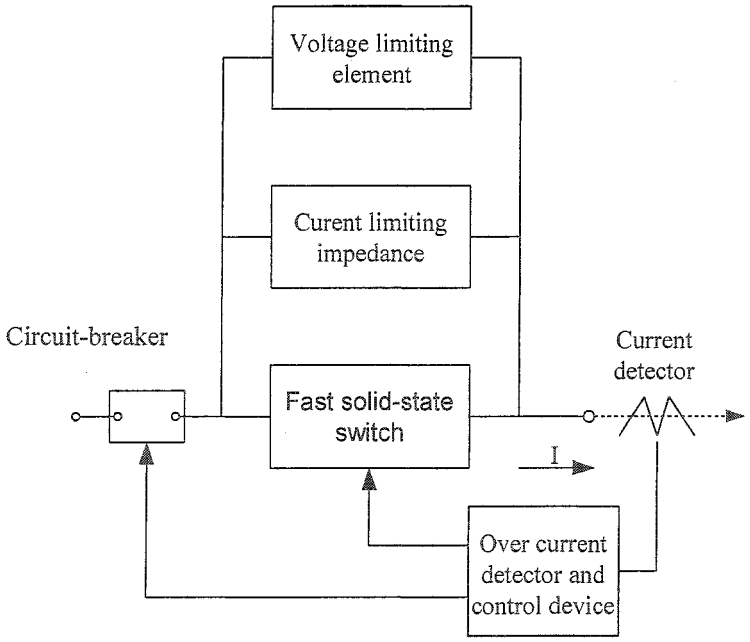


Figure 1.7 Block diagram of the solid-state fault current limiter

1.4.6 Solid-state current interrupter

Figure (1.8) shows the basic configuration of the current interrupting equipment [22]. The equipment consists of, a high-speed vacuum switch (VCB), a fast solid-state switch using GTOs, an overvoltage limiting element (ZnO), a fault detecting circuit comprising an overcurrent and undervoltage detectors, and a control circuit. When a fault occurs in the system, current increases and voltage decreases instantaneously. The fault detecting

circuit detects this state and the control circuit produces a turn-on signal for the GTOs and at the same time an open signal for the VCB. The VCB uses electromagnetic repulsion force to open the contacts at high speed. As a result, an arc is generated between the contacts and an arc voltage appeared in the circuit [23]. The arc voltage acts as counter electromotive force. The fault current flowing into the VCB is reduced by this and commutated to the GTO. When the fault current is completely commutated to the GTO, the GTO interrupts the fault current instantly upon receiving a turn-off signal. Energy remaining in the system is absorbed as heat energy by the ZnO element, which suppresses overvoltages in the circuit.

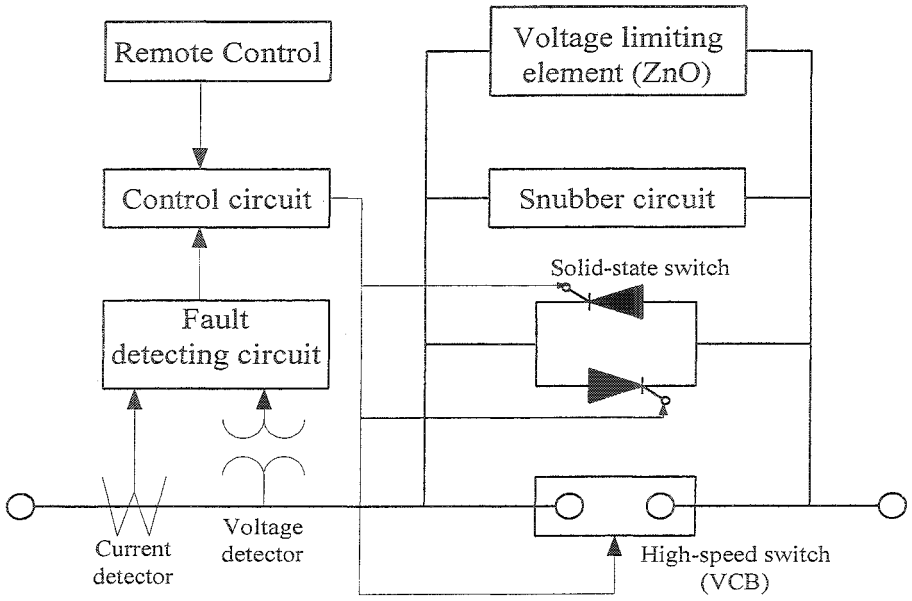


Figure 1.8 Schematic diagram of the solid-state current interrupter

1.4.7 Solid-state circuit-breaker

The Solid-State Circuit-Breaker (SSCB), also referred to as Fault Current Interrupting Device (FCID), is a high-speed switch consisting of two types of semiconductor switches (connected in inverse parallel) and a Varistor, as shown in Figure (1.9). During normal

operations, the semiconductor switches are continuously on. When a fault occurs, the switches are turned off and the fault current is completely interrupted within few ms. The switch is capable of turning off the fault current quickly before it reaches the first peak of the prospective fault current. If the breaker operation is to be co-ordinated with slower downstream protection devices it has to conduct a certain level of fault current for certain period of time. In this case, the current can be immediately transferred to a parallel SCR switch with a current limiting reactor. The thyristor branch has a current control loop for limiting fault current for long periods and can thus reduce the size of reactor size.

Advantages of SSCB:

- The SSCB offers a viable solution to most of the distribution system problems that result in voltage dips, swells and power outages.
- The SSCB can instantly isolate any part of a network, which is experiencing a fault from another healthy part. Thus, maintaining a high quality of supply to the healthy part.
- The SSCB can instantly transfer sensitive loads from a normal supply that experiences a disturbance to an alternative supply that is unaffected by the disturbance.
- The SSCB act as an extremely fast transfer switch that allows the resolution of supply to the load within ¼ cycle. A 13 kV prototype SSCB was commissioned in 1995 for

Public Service Electric & Gas Co., USA. [24].

Drawback with SSCB

- Continuous conduction losses, which increase cooling cost.

It is not fail safe device. That is in case of any switch failed (short-circuit) it could lead to

a more serious damage. since the device is not fully protected.

- Resonance during FCL mode.

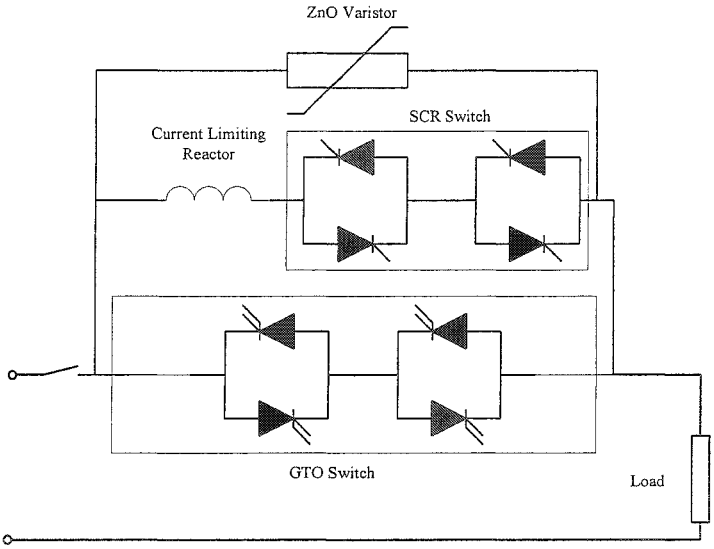


Figure 1.9 Solid-state circuit-breaker

1.4.8 Current controlled current limiting device

The basic configuration of the current controlled current limiting device is shown in Figure (1.10). The principle of operation of this device is based on the principles of the thyristor controlled reactor [25]. When a fault is detected the first peak of the fault current is limited by instantly turning off the semiconductor switch (IGBT). Then the firing of the thyristors is delayed by at least 90 degrees after zero crossing of the voltage waveform. The fault current is measured and used for the correction of the firing angles for subsequent firings. If the adjusted firing angle less than a pre-set value (60-70 degrees) this is interpreted as there is no more need for limitation of the fault current and the control is switched back to normal operation. Based on the junction temperature calculation of the IGBT, the maximum operation of this device is limited 100 ms. Which

result in lack of co-ordination. The second disadvantage is that the level of the limited fault current depends upon the firing angle and the value of the inserted inductance.

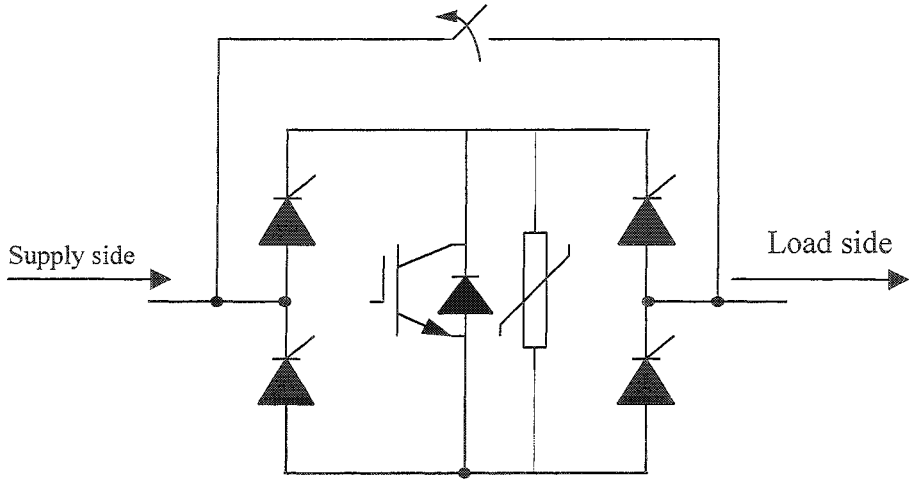


Figure 1.10 Current controlled current limiting device

1.5 The Fault Current Limiting and Interrupting Device

The structure of the proposed fault current limiting and interrupting device (FCLID) is shown in Figure (1.11) [26]. It consists of a high speed, bi-directional switch realised using power semiconductor devices such as IGBTs, a varistor (non-linear resistor) and a snubber circuit, all connected in parallel.

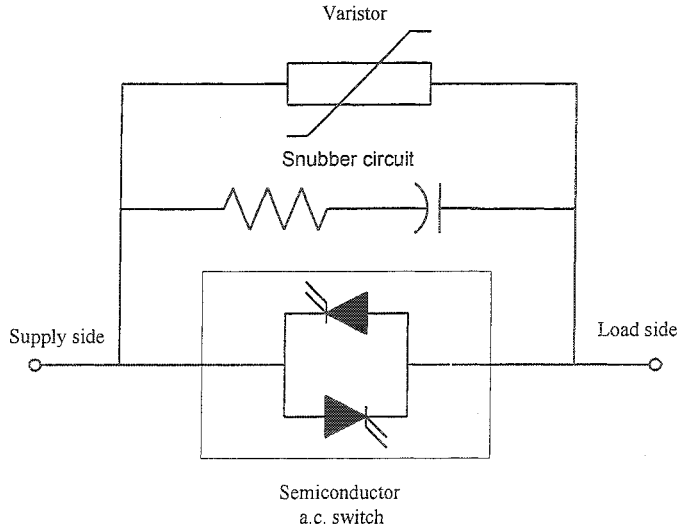


Figure 1.11 Fault current limiting and interrupting device

In normal operation, the semiconductor devices are constantly turned on. Alternatively, the whole FCLID can be bypassed using a vacuum circuit-breaker to avoid losses. The bypass circuit-breaker is opened when the FCLID is required to operate.

Assuming that a short-circuit fault occurs on the load side, a semiconductor device will initially conduct the fault current. As shown in Figure (1.12), the switch is turned off when the fault current reaches a preset value Imax which should be within the interrupting capability of the semiconductor device. The fault current is thus diverted to the varistor. The clamping voltage of the varistor is set to be higher than the peak supply voltage. Therefore, the current in the faulty circuit starts to decrease. The varistor voltage is almost constant as long as it is conducting. When the current reduce to pre-set value Imin, the semiconductor device is turned on again to re-establish the current. Switching is continued for both positive and negative half cycles of the fault current and the operation is maintained for a specified period of time, which is useful for protection co-ordinate. If the fault persists, the semiconductor devices are turned off permanently, after certain time, and the fault current is completely interrupted.

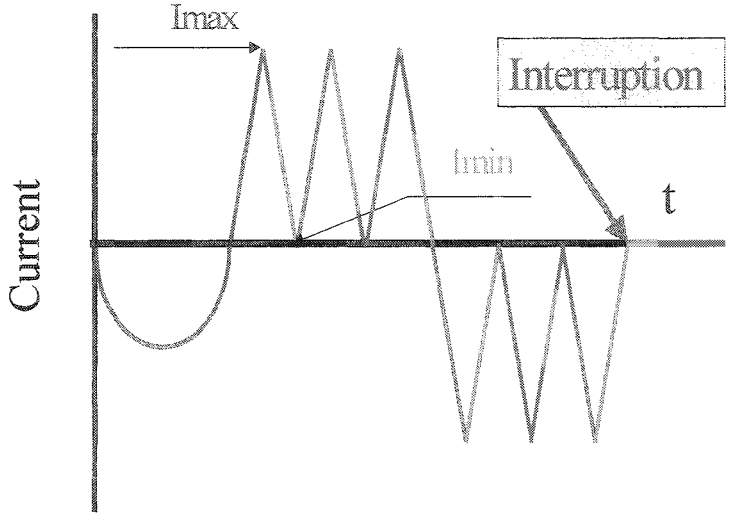


Figure 1.12 Current waveform

Characteristics of the FCLID

The FCLID has the following features that makes it better suited than conventional devices to the duty required. These features enable the development of a "smart" device which is capable of automatically adjusting its operation (e.g. switching pattern) to suit the device and the distribution network requirements (e.g. protection co-ordination).

- The configuration and control scheme of the FCLID enable flexible and fully controllable operation for both functions, i.e. current limiting and interruption.
- The FCLID allows for the effective value of the fault current to be controlled to suit the system requirements. In addition, unlike other FCLD, the fault current level during the operation of the device is independent of the system impedance or the fault location. This can assist in setting protection co-ordination within the distribution network.
- The FCLID offers improved performance, including very fast response, ability to limit the fault current to within safe limits and a long multi-operation life span. It also offers the advantage of not requiring active cooling. In addition, it offers the ability to switch the power line ON and OFF via a remote control signal. It can also be designed to do a self-testing routine periodically, thus its reliable operation can regularly be checked and maintained.
- The period of operation of the FCLID is controllable which makes the device immune to nuisance tripping caused by transformer or capacitor inrush current, network switching, etc. This makes it easier to incorporate the device with other relay protection schemes.
- The deployment of varistors across the solid-state switching components facilitates

series connection of IGBTs, which is necessary for high voltage applications, e.g. 11 kV.

The drawbacks of the FCLID are as follow:

- The nature of operation of the FCLID imposes very server stresses on the semiconductor device and the varistor. The semiconductor device must be switched off before reaching Imax. The power dissipation in semiconductor device and the varistor must be adequately assessed and their temperature properly monitored and kept within safe limits.
- The varistor is not designed for continuous repetitive pulses, a suitable method need to be developed to evaluate the energy handling capability of the varistor under repetitive pulses. In addition, the energy handling capability of the varistor is limited and parallel operation is needed to achieve the FCLID, due their nonlinear characteristics, it is difficult to match the characteristics of parallel devices. A suitable method need to be developed to improve current sharing between parallel elements.
- Harmonics produced by the FCLID may create problems; mainly that of resonance at certain operating conditions. A suitable control technique need to be developed to avoid damage to other equipment.

This work investigates the above drawbacks and suggests possible solutions.

1.6 The Objectives of This Research

The research reported in this thesis describes the development of a solid-state Fault Current Limiting and Interrupting Device suitable for power distribution networks.

The main objectives of the research are:

- Study and analyse the dynamic behaviour of the GTO, IGBT and IGCT in order to

find a suitable switch for this application. Also, to fully utilise the capabilities of the selected switch for the FCLID application.

- Investigate and analyse the suitability of commercially available varistors for this application. This includes the study of electrical characteristics, failure modes and energy handling capability of varistors under continuous repetitive pulses.
- Develop a simulation model for the proposed FCLID using MATLAB/SIMULINK and analyse its performance. The FCLID model is incorporated in a typical distribution network and its effects on the network are analysed.
- Investigate the problem of harmonics associated with the FCLID and develop a suitable control technique to ensure optimal performance during fault conditions.
- Develop a 230 V prototype model of the FCLID and a test rig to evaluate the performance of the FCLID and its effectiveness when used with sensitive loads such as switched mode power supplies.
- Establish the outline design specification of a FCLID suitable for 11 kV distribution networks.

1.7 The Structure of The Thesis

The thesis is structured into the following:

CHAPTER ONE: gives an overview of fault current limiting and interrupting devices and their applications in power distribution networks. It also describes the principle characteristics of the proposed fault current limiting and interrupting device and presents its characteristics.

CHAPTER TWO: describes the computer simulation of the proposed FCLID and its implementation into a typical distribution network. The performance of the FCLID and its effects on the power quality are also presented.

CHAPTER THREE: gives an overview of semiconductor switches suitable for implementing in the FCLID. A thermal model of the selected switch is developed and the rise in junction temperature is calculated to define the maximum operating time of the FCLID. Finally, a new method for predicting the IGBT junction temperature under transient conditions is presented.

CHAPTER FOUR: gives an overview of the varistor electrical characteristics, microstructure and failure modes. It also presents the method developed in this work to evaluate the energy handling capability of metal oxide varistors. Finally, a method is proposed for improving the current sharing between parallel varistor to achieve the energy rating required for developing the FCLID.

CHAPTER FIVE: describes the design and construction of an experimental prototype fault current limiting and interrupting device. Details of the controller, peripheral circuits (snubber, gate drive, current measurement and protection) and construction of the test rig are presented. Test results for the FCLID operation under different operating conditions are presented. Finally, a practical implementation of the FCLID and design specifications of the 11 kV FCLID are presented.

CHAPTER SIX: gives analysis of harmonics associated with FCLID operation, their causes, effects and applicable standard. Harmonics produced by the proposed FCLID are evaluated and solutions to reduce their level in the system are suggested. Finally, the

effects of the FCLID on the operation of sensitive loads, such as switch mode power supplies are analysed.

CHAPTER SEVEN: presents the conclusions drawn from the experience gained during this work and suggestions for future work.

1.8 Original Contributions

The research carried out in this work has resulted in the following contributions to the knowledge:

1. A criterion to determine the stress on the IGBT and varistor for this type of application has been developed.
2. An alternative technique for measuring the energy handling capability of ZnO varistors under continuous repetitive pulses has been investigated and developed.
3. A method for improving current sharing between parallel varistors is proposed.
4. A new method for predicting the junction temperature of a solid-state switch under transient condition has been developed.
5. A novel method for predicting the varistor temperature under repetitive pulses has been developed.
6. Development of an experimental FCLID prototype.

These contributions are supported by the following publications.

[1] M.M.R. Ahmed, and G. Putrus, "Investigation into custom power technology" Proceeding of the 34th University Power Electronics Conference, Leicester, UK, 1999, Vol. 2, pp. 519-521.

[2] M.M.R. Ahmed, G.A.Putrus, L.Ran and L.Xiao, "Harmonic analysis and improvement of a new solid-state fault current limiter," Proceedings of the 45th IEEE Rural Electric Power Conference, Little Rock Arkansas, USA, 2001, pp. D.5.1-D.5.8.

[3] G.A.Putrus, L.Ran and M.M.R. Ahmed, "Improving the current sharing between parallel varistors", Proceedings of the IEEE International Symposium on Industrial Electronics, Pusan, Korea, 2001, Vol. 2, pp. 1324-1327.

[4] M.M.R. Ahmed, G.A. Putrus, L.Ran and R. Penlington, "Measuring the energy handling capability of the metal oxide varistor," Proceedings of the 16th International Conference on Electricity Distribution, Amsterdam, Netherlands, 2001, pp. 1.33.1-1.33.5.

[5] M.M.R. Ahmed, G.A. Putrus and L.Ran, "Predicting IGBT junction temperature under transient conditions", Proceedings of the IEEE International Symposium on Industrial Electronics, L' Aquila, Italy, 2002, pp. 100-1-100-4.

[6] M.M.R. Ahmed, G.A. Putrus and L. Ran, "Power quality improvement using a solid-state fault current limiter", Accepted for presentation in the IEEE/PES Transmission and Distribution Conference, Yokohama, Japan, October 6-10, 2002.

[7] M.M.R. Ahmed, G.A. Putrus and L.Ran, "Development of a solid-state fault current limiting and interrupting device suitable for low voltage distribution networks", prepared for publication in IEEE Transactions on Power Delivery.

[8] A patent application has been filed.

CHAPTER TWO

SIMULATION WORK

2.1 Introduction

Computer simulation is a very powerful tool, when appropriately used can effectively demonstrate many facts of new applications. This research uses computer based analysis and design, through software modelling, as an illustrative tool to establish the key factors concerned with using solid-state technology in the development of the FCLID. Simulation allows the design, operation of the FCLID and its effects on electric power distribution to be analysed.

THIS CHAPTER gives an overview of the software packages available for modelling and analysis of the FCLID. The software used in this work is MATLAB/SIMULINK with its POWER SYSTEM Blockset. The developed computer model of the FCLID is implemented into a typical distribution network and its performance under different operating conditions is analysed.

2.2 Software Packages for FCLID Simulation Development

Historically, simulation of a transient phenomena related to power systems has been carried out using the electromagnetic transients program (EMTP) [27] or one of its variants, such as the alternative transient program (ATP) or electromagnetic transients for dc (EMTDC). All of these program are based on the trapezoidal integration rule and the nodal approach. These software packages use fixed step algorithms, which yields excellent results for power systems free of power electronics switching devices. However, the fixed-step algorithms do not adapt well to the presence of discontinuities

that are caused by the switching devices. SPICE is another simulation program for general-purpose circuit analysis, which was developed at the University of California, Berkeley [28]. It contains models for basic circuit elements (R, L, C, sources, etc.), switches, and most common semiconductor devices (diodes, transistors, MOSFETs, IGBT's, etc.). SPICE is mainly used to simulate electronic circuits for analysis such as d.c., a.c., transient, sensitivity and noise. It uses the nodal approach with variable time-step integration algorithm so that it can correctly simulate switching electronic circuits. The simulation of control systems in PSPICE (a commercial version of SPICE) is facilitated by using the Analogue Behaviour Modelling (ABM) Blocks. However, there are no specific models for power systems and drives, such as electrical machines and control circuits. To build these models using SPICE basic elements, the simulation setup becomes highly time consuming; if not impossible. MATLAB/SIMULINK software package with POWER SYSTEM Blockset [29,30], is a convenient tool to simulate electric circuits containing power electronic devices, since it detect very accurately the instant at which discontinuities and switching occur. Also the user can easily integrate control and power systems within Simulink environment. In addition, the user has access to numerous design and analysis tools provided in Matlab and its toolboxes. Further more, this software offers the following:

- Simulink's variable-step event sensitive integration algorithms allow increased accuracy in zero-crossing detection of current as compared with (non-interpolated) fixed-step algorithms.
- Simulation either with continuous variable time-step integration algorithms or with discretized system is possible. For large systems, which contain many states or many

nonlinear blocks such as power electronic switches, discretization of the electrical system allows much faster simulation than variable-step methods.

- Simulink's graphical interface provides a user-friendly environment where the power circuit and control system are represented in the same diagram. Results may be displayed while the simulation is running.
- The processing power of MATLAB allows the designer to perform a complex post-processing on simulation results.

2.3 FCLID Computer Model

Modelling the FCLID including the power network and its controller in Simulink environments requires "electric blocks" from the Power System Blockset and control blocks from Simulink library. The model of the developed FCLID is shown in Figure (2.1). It has three functional blocks, power circuit, full wave rectifier and controller with two switching logic blocks one for the positive and one for the negative half cycle. The FCLID power circuit consists of two IGBTs, two diodes RC snubber circuit and a varistor as shown in Figure (2.2). The IGBT model is composed of ideal switch associated with R, L components and logic functions that control the switching characteristics of the device. The varistor model consists of three exponential terms, which are selected to fit with the actual characteristics obtained from manufacturer's data sheet. The controller diagram shown in Figure (2.3) it consists of three comparators, a timing circuit and a D flip-flop.

To realise the FCLID characteristics, two control variables are of concern as shown in Figure (2.3). One is the maximum instantaneous fault current at which the switch is turned-off (Imax).

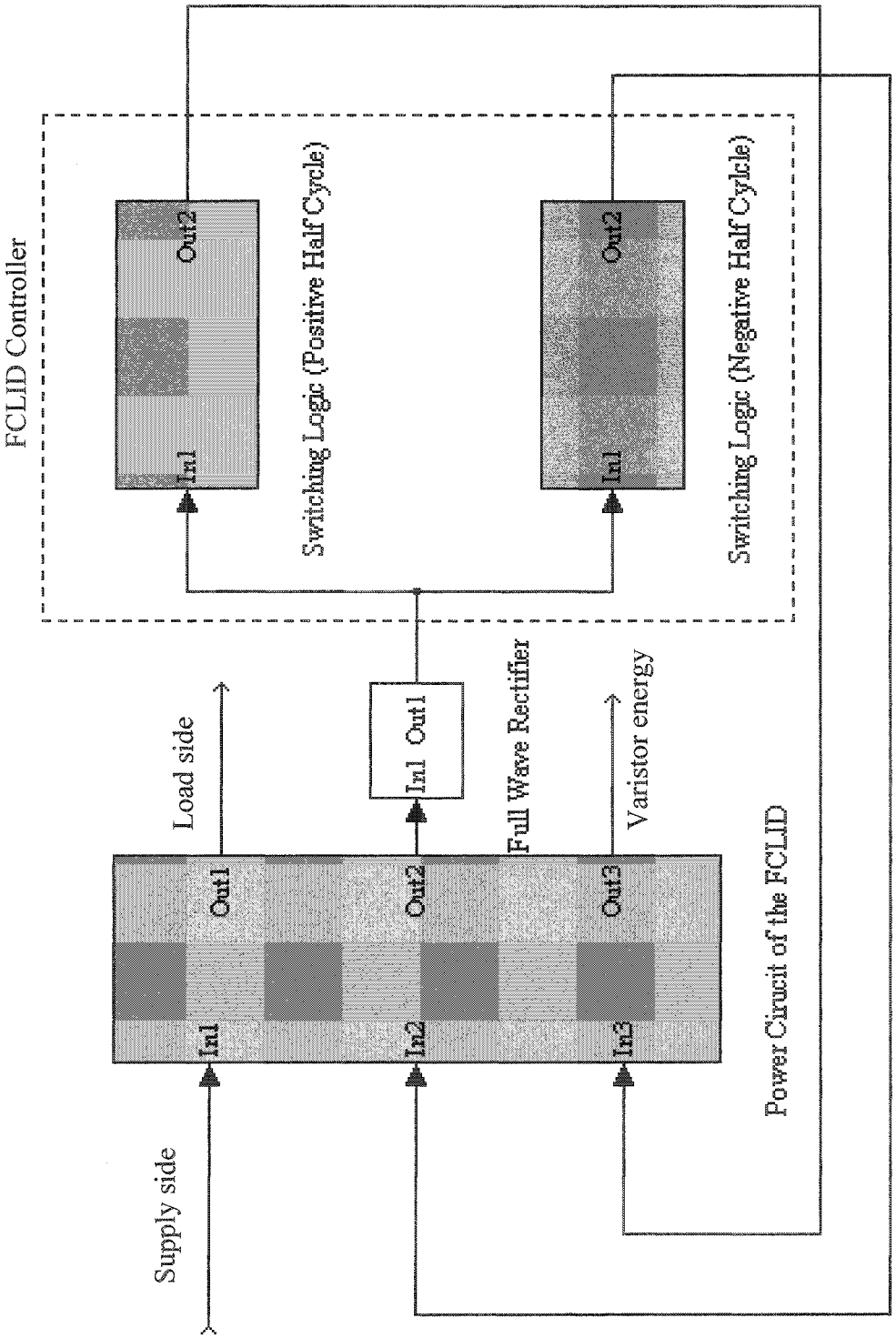


Figure 2.1 A block diagram showing the main components of the FCLID model

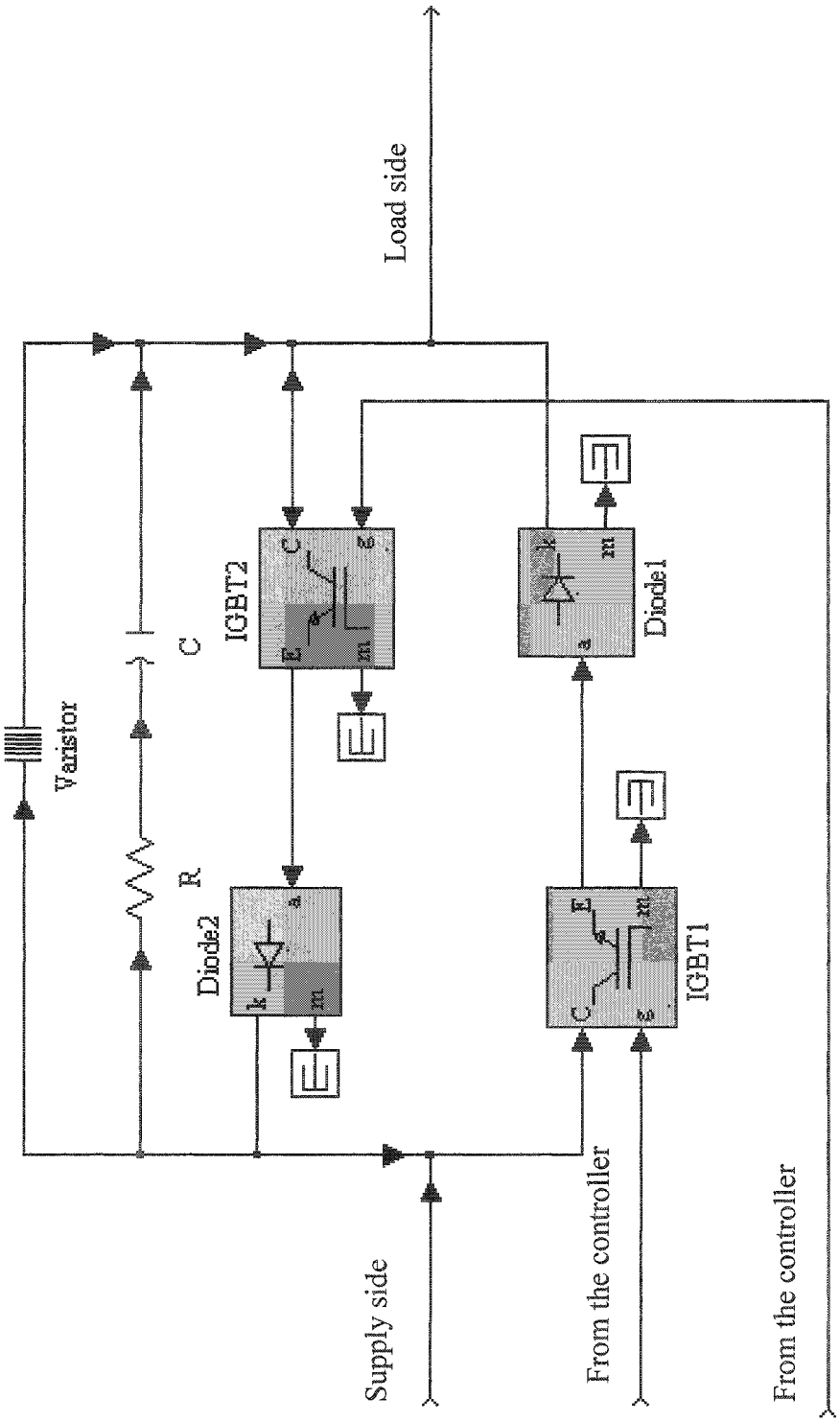


Figure 2.2. The Power circuit of the FCLID model

The second is the minimum value at which the switch is turned-on after every current interruption (Imin). The value of Imax depends upon the semiconductor switch turn-off capability and should allow a sufficient time from the instant the fault occurs to the instant when the fault current is detected and interrupted, taking into account the normal operating current.

When the switch is turned off, the current through the varistor increases rapidly to a maximum peak value equal to Imax. Then the energy trapped in the system impedance start to dissipate into the varistor and voltage across decrease as long as the switch is OFF. Due to the high non-linear characteristics of the varistor, the current through it decays rapidly. When the switch turned on at Imin the circuit current start to increase with the rate determined by the system impedance and the circuit initial conditions. Therefore, to set the minimum current at which the switch is turned on (Imin), one technique has been chosen to fix Imin and to let the frequency of the switch change.

2.4 Simulation Results

To illustrate the FCLID operating principles, a simulation model of the FCLID is tested in a typical 230 V distribution network model shown in Figure (2.4). The pre-fault total load current is assumed to be less than 40 A. Without the fault current limiter, the prospective peak short-circuit current for a single line to ground fault at the busbar of Load 4 is 1 kA. The value changes to 2 kA, 3 kA and 4 kA for faults at Load 3, Load 2 and Load 1, respectively.

The maximum through current when using the FCLID is set to Imax=120 A. For the case of a fault at load 4, Figure (2.5) shows the current through the FCLID and voltage waveforms at the PCC without the FCLID (voltage angle at fault instant was 90^{o}).

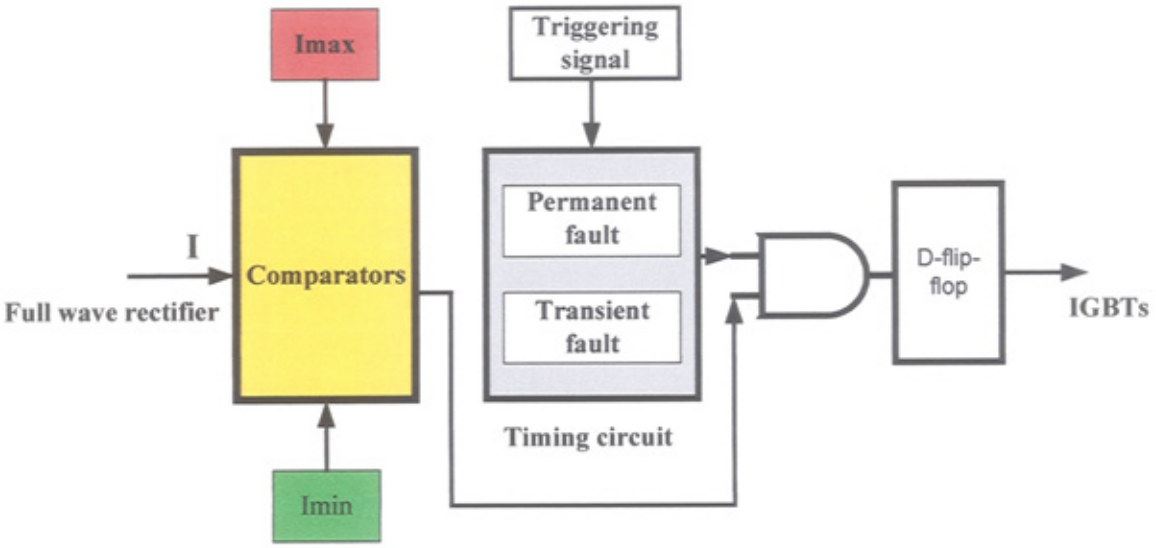


Figure 2.3 Detail of the FCLID controller

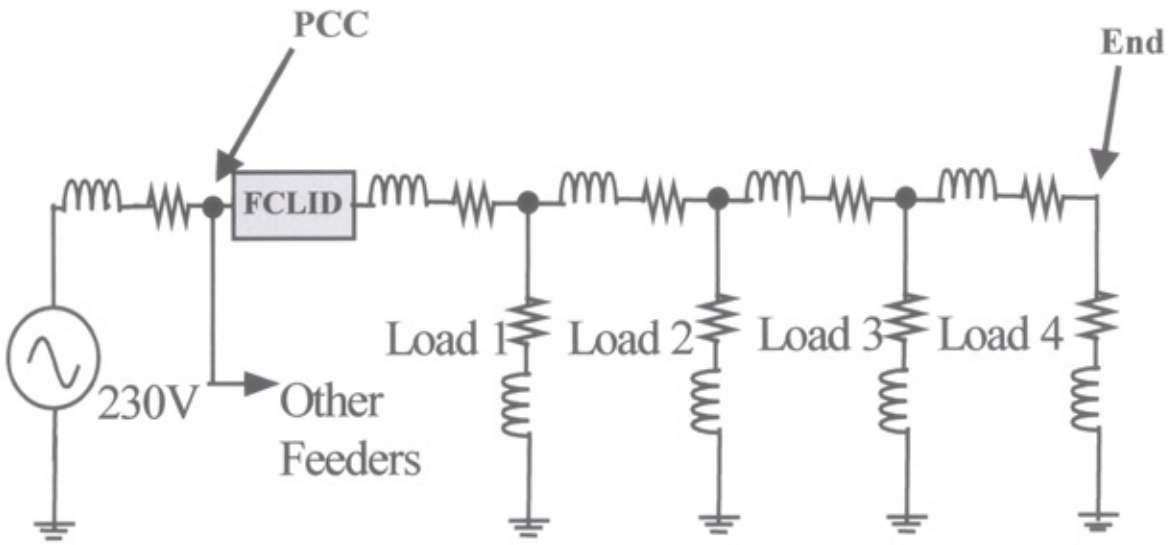
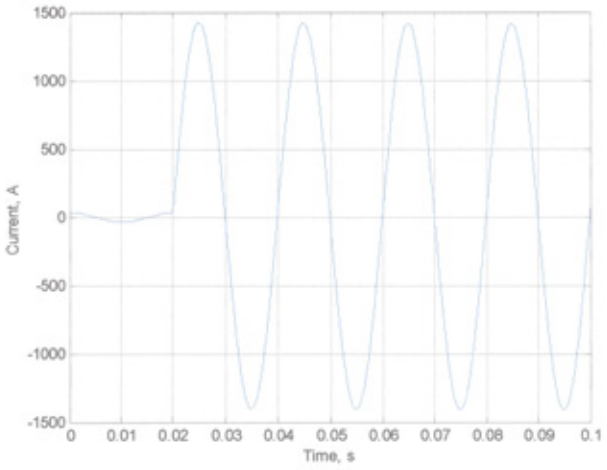
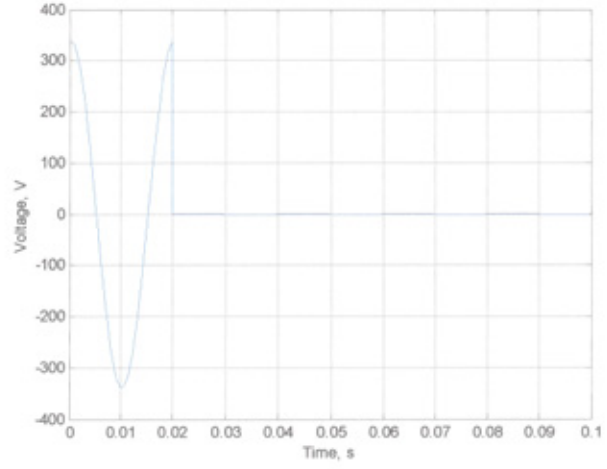


Figure 2.4 FCLID incorporated in a typical distribution network

Figure (2.6) shows the current and voltage waveforms with the FCLID installed in the network. Imin is set to 0A in this case. Figure (2.7) illustrates the current waveforms (with and without the FCLID) for short-circuit current level of 1 kA. As can been seen the FCLID has limited the current to 120 A peak with Imin = 0 A. The simulation results demonstrate a fault occurrence at 0.02 s, FCLID ability of limiting the current for 0.06 s and a complete current interruption at 0.08 s. As will be shown later, the developed experimental model of the FCLID can limit the fault current for up to 0.8 s.

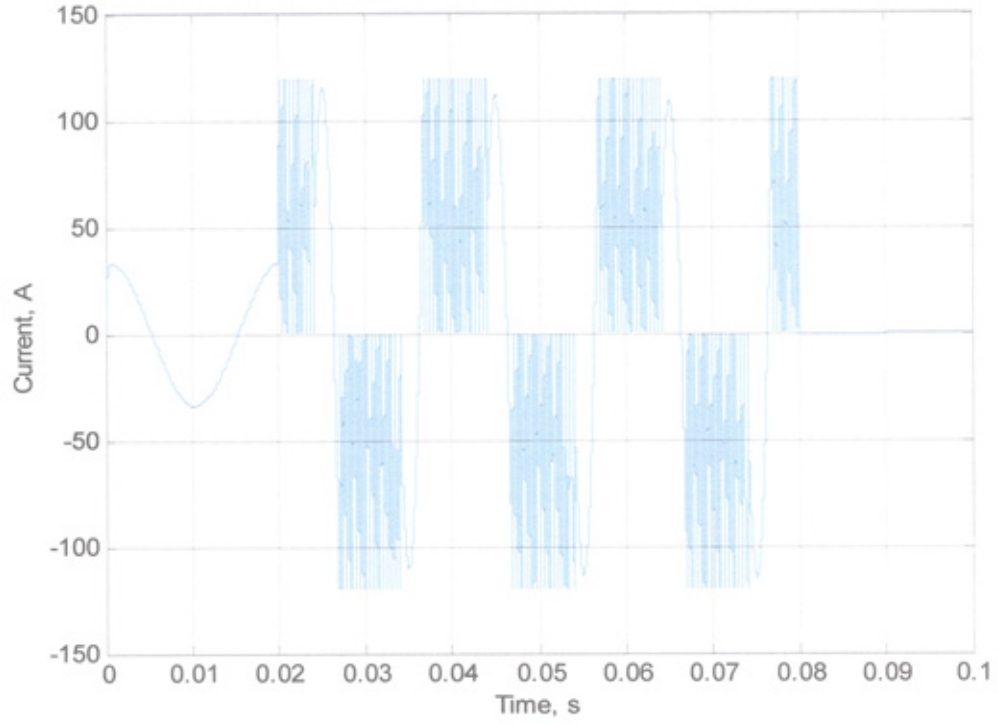


(a)

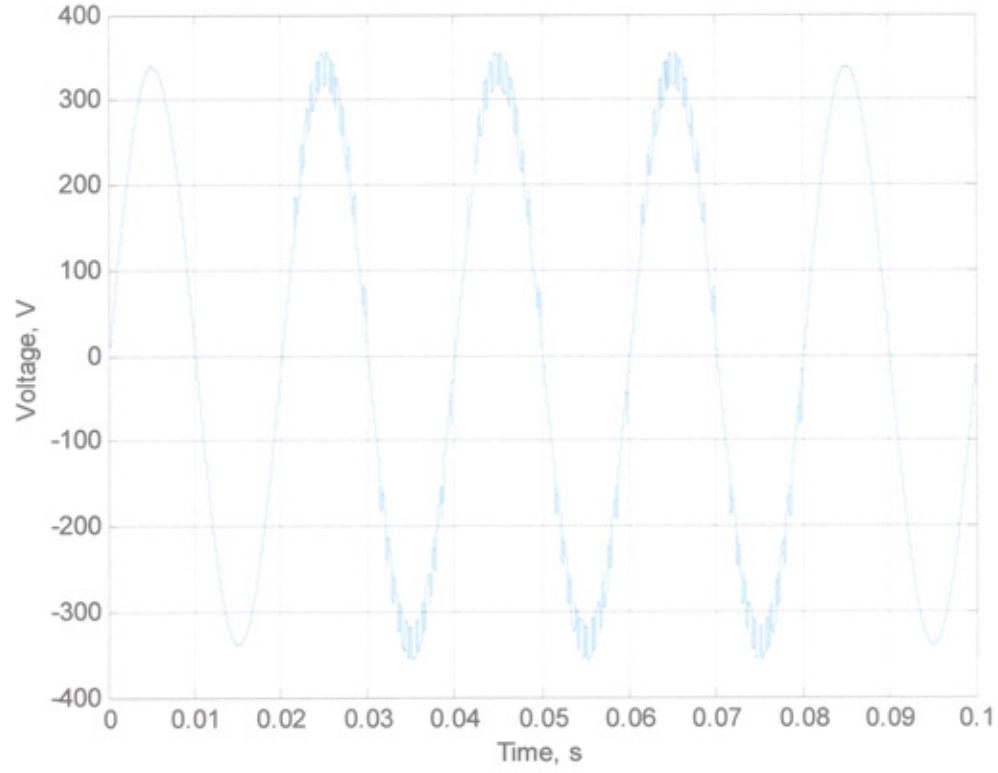


(b)

Figure 2.5 Current and voltage waveforms without FCLID



(a)



(b)

Figure 2.6 Current and voltage waveforms with FCLID

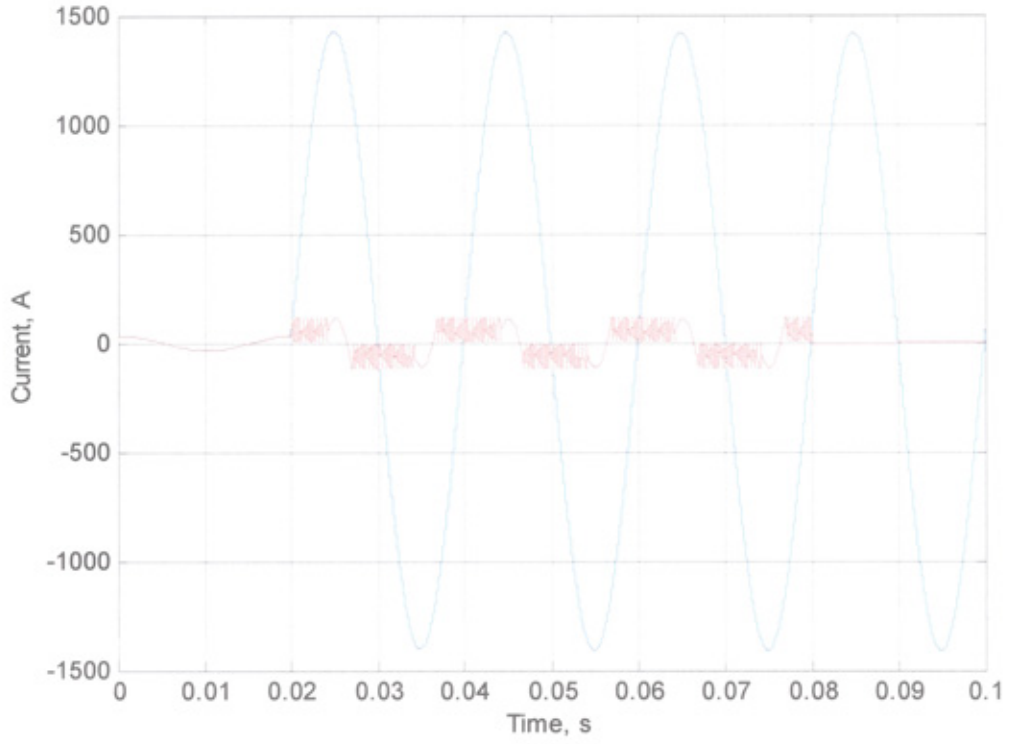


Figure 2.7 Current waveforms with and without FCLID

As may be noted from the current waveform, the FCLID will produce a substantial amount of harmonic currents in the fault path. These currents may create problems in power systems; mainly that of resonance at certain operating conditions. This problem will be analysed in details in Chapter 6.

To reduce harmonics and increase the r.m.s. value of the limited current to allow co-ordination with the other protection devices, Imin should be higher than zero. So increasing Imin or short-circuit level will lead to over stress on both the switching device and varistor.

In order to define the effects of changing Imin and short-circuit level on the switching device and varistor, a new criterion is developed to define the stress on the FCLID components (switching device and varistor).

2.5 Effects of Operating Conditions on The FCLID

For investigating the FCLID performance under different operating conditions (Imin & short-circuit level), analytical & computer models for the FCLID were developed where the stress on the FCLID main components could be calculated based on various parameters of the network (see APPENDIX A).

Figure (2.8) gives the relationship between the energy input to the varistor during 20 ms of the FCLID operation and the short-circuit level (Imin = 0 A). The effect of the fault level on the switching frequency is shown in Figure (2.9). These results show that as the short-circuit level increases the IGBT losses increase while the energy dissipated in the varistor is almost constant.

Figure (2.10) shows the varistor energy dissipation as a function of Imin. Imax is set to 120 A. As Imin increases the average varistor current increases and so does the energy dissipation. Figure (2.11) shows that the average switching frequency of the FCLID increases with Imin. It is clear that as Imin increases both the IGBT switching losses and the varistor energy loss increases.

It can be observed from Figures 2.8 and 2.10 that there is little difference between the calculated and simulated energy values. This mainly results from the assumption of the varistor clamping voltage being almost constant (actually there is a slight decrease in the clamping voltage during the turn-off period of the solid-state switch).

It can be noticed from the results in Figures 2.9 and 2.11 that there is a good agreement between the calculated switching frequency and that obtained from the simulation at lower current levels. The small differences at higher Imin values are due to the constant pulse width assumption (in reality this is variable).

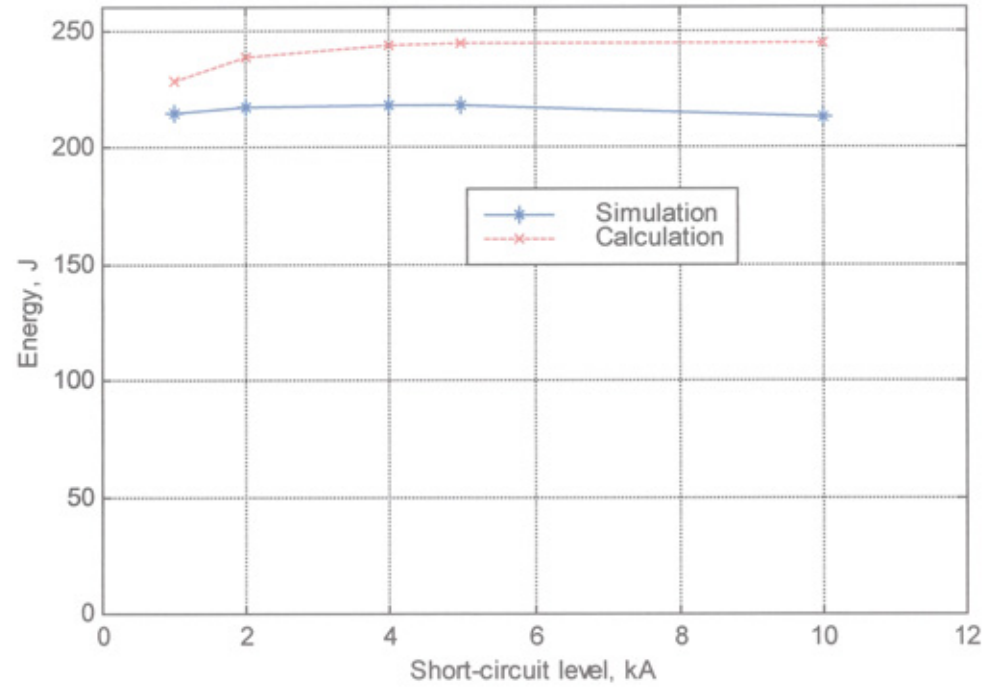


Figure 2.8 Relationship between the energy input to the varistor and short-circuit level

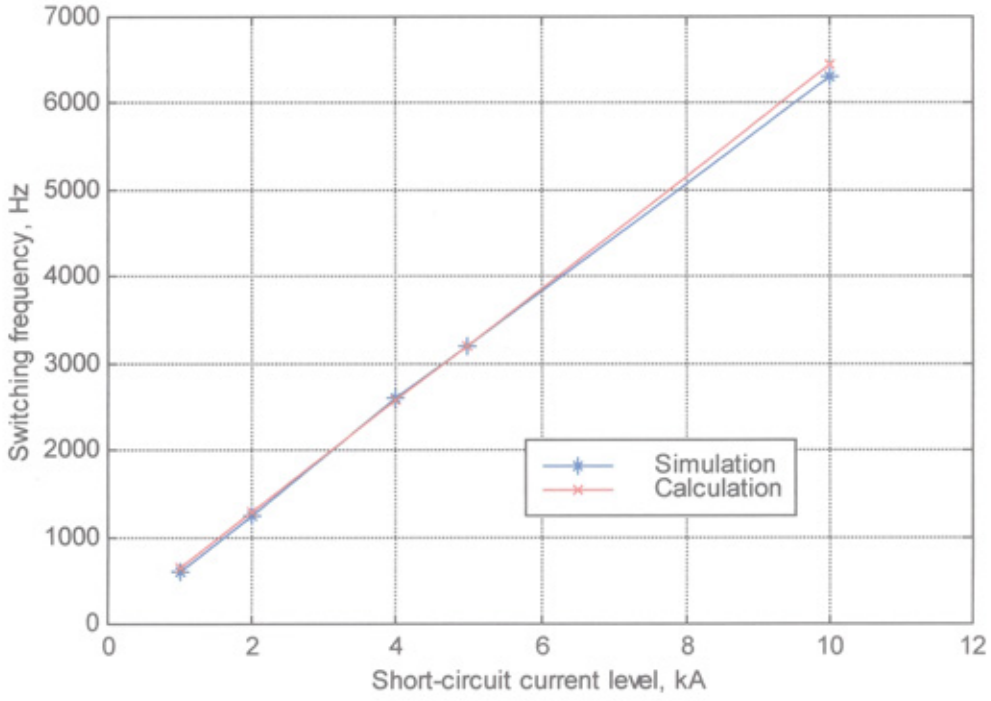


Figure 2.9 Relationship between switching frequency and short-circuit current level

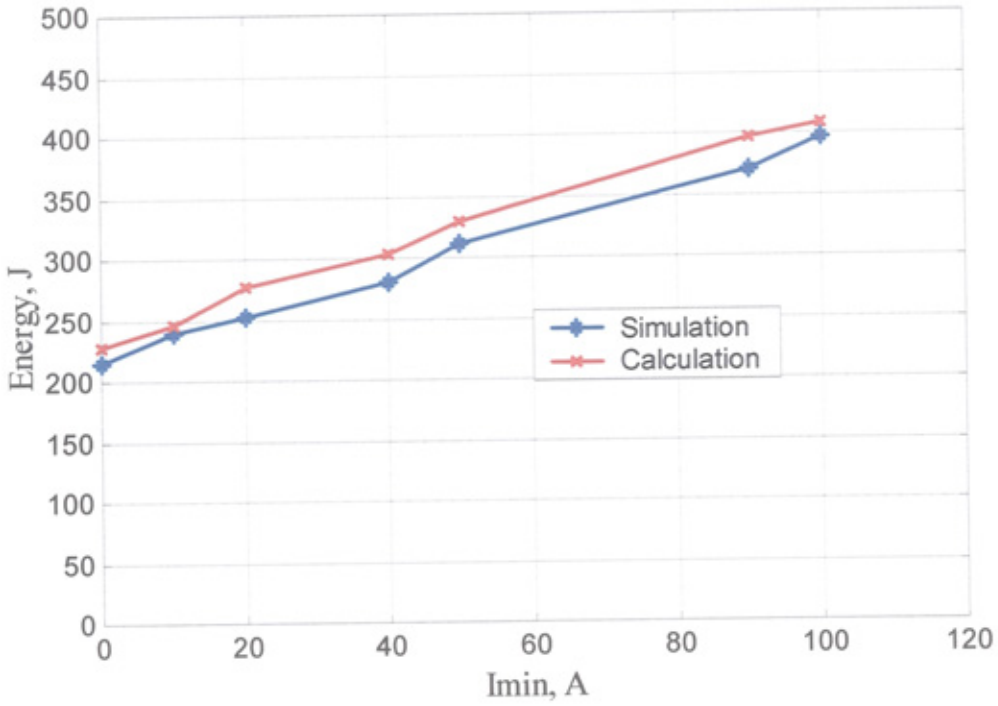


Figure 2.10 Relationship between the energy input to the varistor and Imin

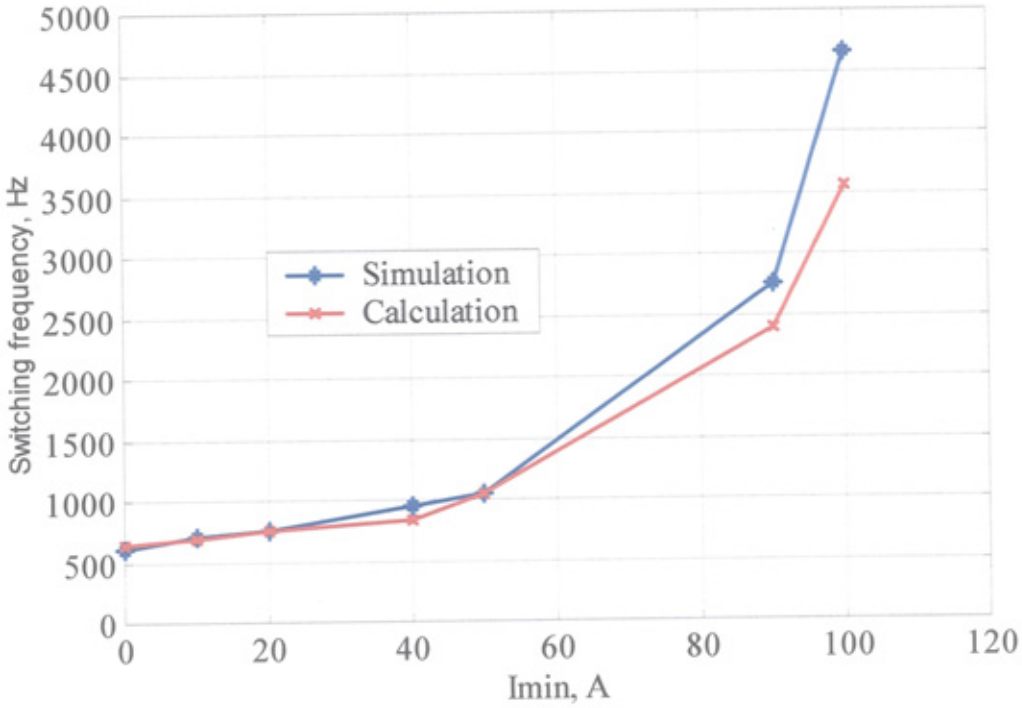


Figure 2.11 Relationship between switching frequency and Imin

2.6 Simulation Results of a Three-Phase System

The performance of a typical radial distribution system with and without the FCLID under different fault condition was tested using MATLAB/SIMULINK and POWER SYSTEM Blockset. The three-phase system consists of a source, an 11 kV / 433 V Δ / Y transformer, a RL branch representing the cable impedance and a load. Figure (2.12) shows the three- phase model of the radial distribution network with the FCLID.

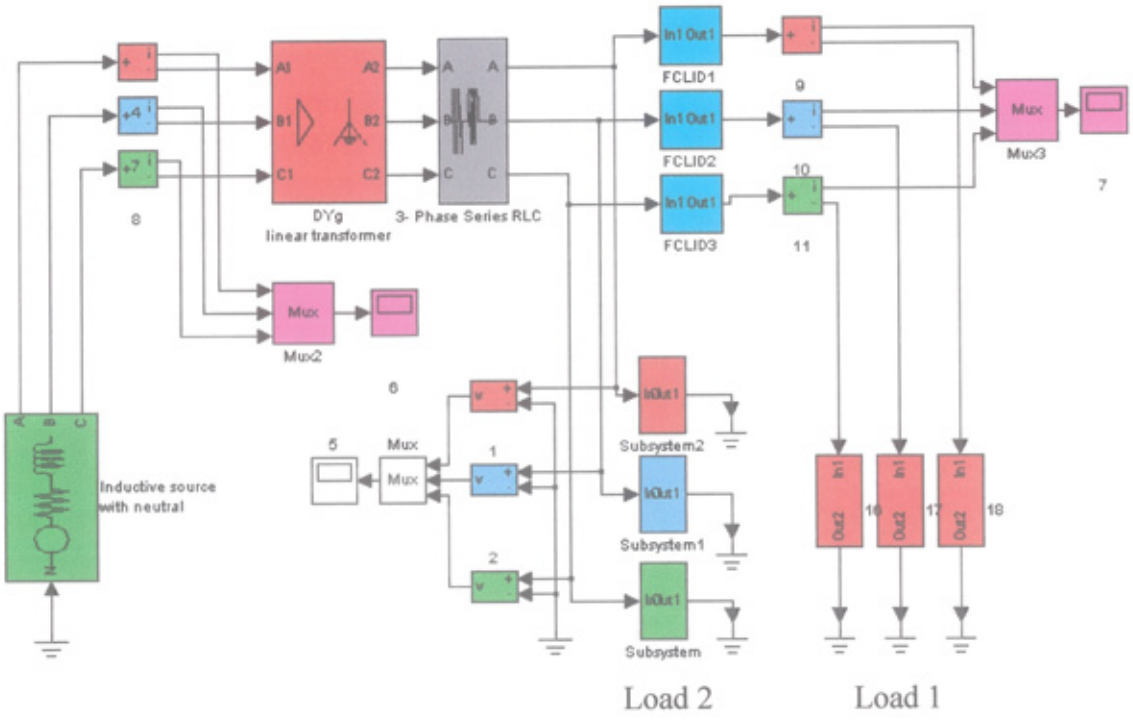


Figure 2.12 Three phase model of a radial distribution network with FCLID

Single line to ground fault

A single line to ground fault is created in an effectively grounded distribution system shown in Figure (2.12). Figures 2.13 and 2.14 present the current and voltage waveforms at the secondary side of the transformer when the FCLID is not implemented.

Figures 2.15-2.17 illustrate the simulation results for a single line to ground fault (phase a) when the FCLID is implemented. Figures 2.15 and 2.16 show the current and voltage

waveforms at the secondary side of the transformer and Figure (2.17) the primary side current waveforms. It can be seen from Figure (2.17) that the primary line current Ic has no ripple at all this resulting from modelling the 3 - phase transformer using three 1-phase transformers (there is no magnetic coupling between different phases).

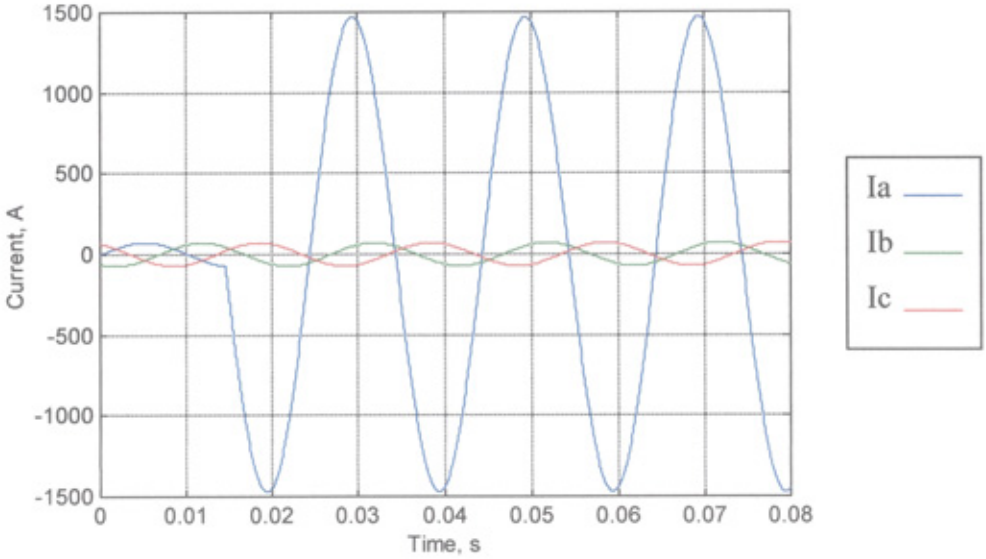


Figure 2.13 Current waveforms during a 1L-G fault without FCLID

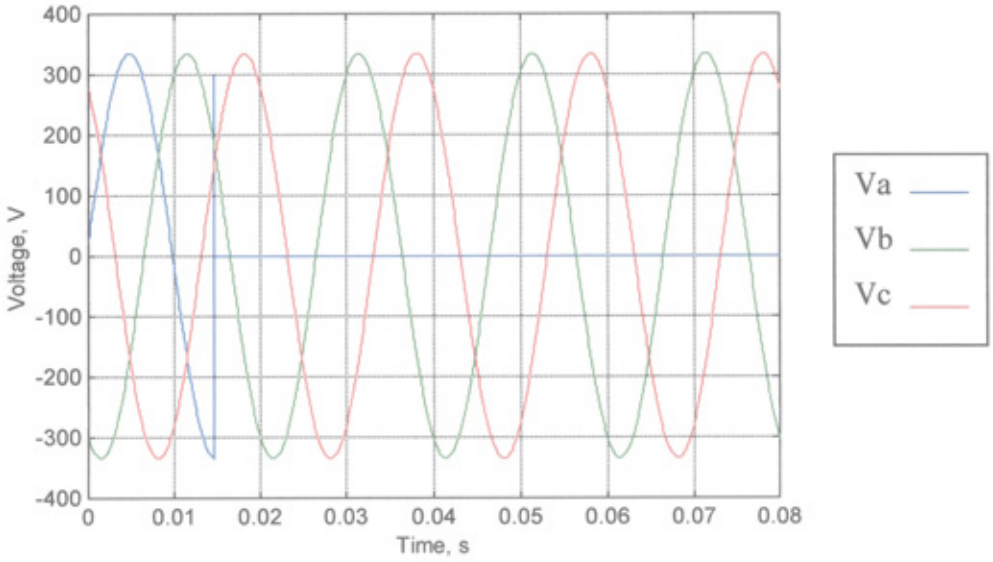


Figure 2.14 Voltage waveforms during a 1L-G fault without FCLID

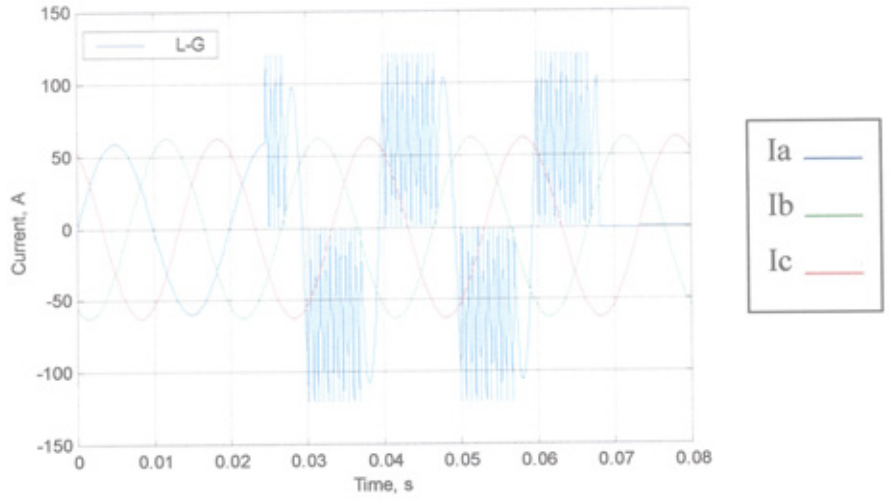


Figure 2.15 Current waveforms during a 1L-G fault with FCLID

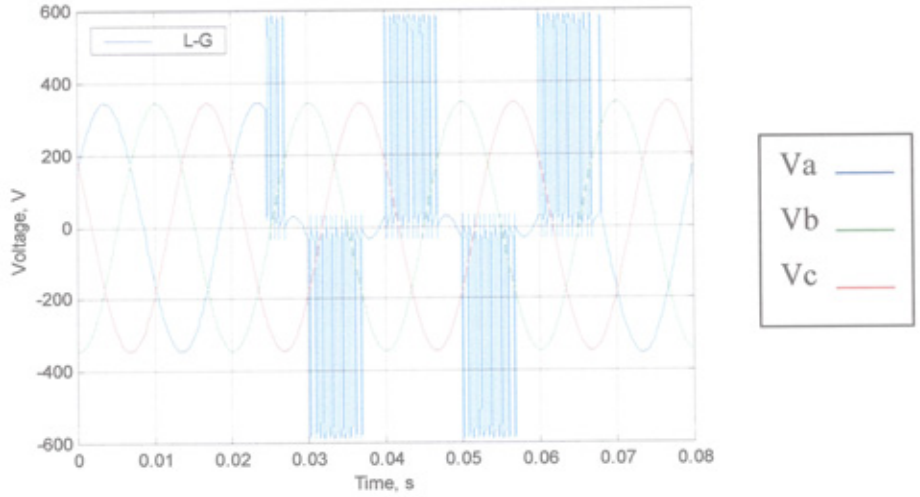


Figure 2.16 Voltage waveforms during a 1L-G fault with FCLID

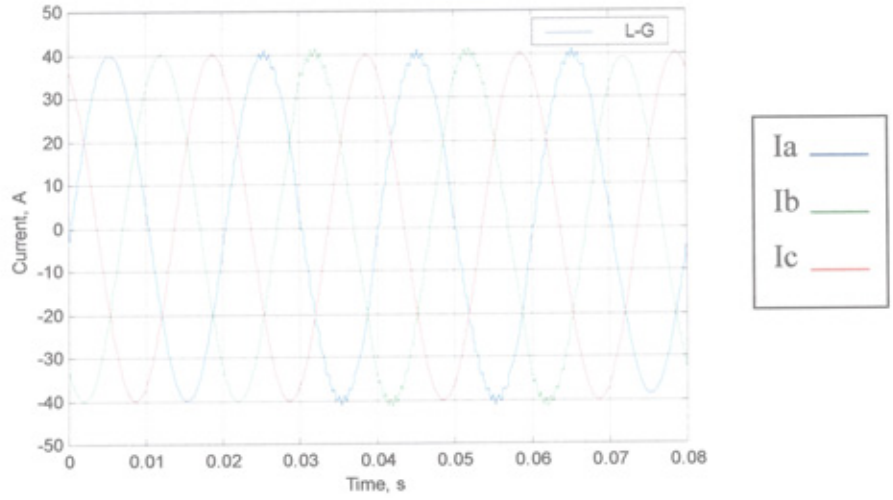


Figure 2.17 Current waveforms during a 1L-G fault with FCLID

Double line to ground fault

The current and voltage waveforms at the secondary side of the transformer for a double line to ground fault are shown in Figures 2.18 and 2.19.

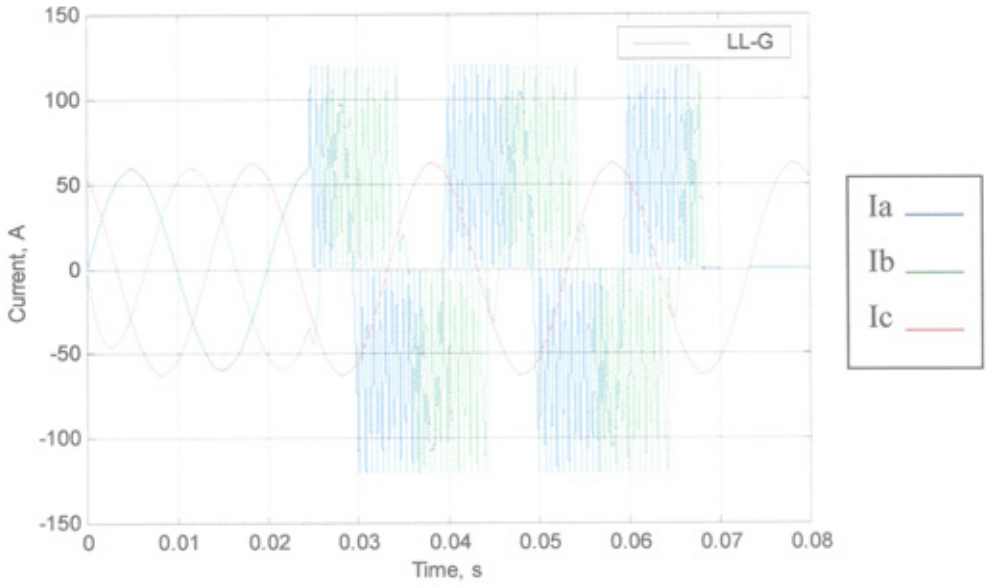


Figure 2.18 Current waveforms a L-L-G during fault with FCLID

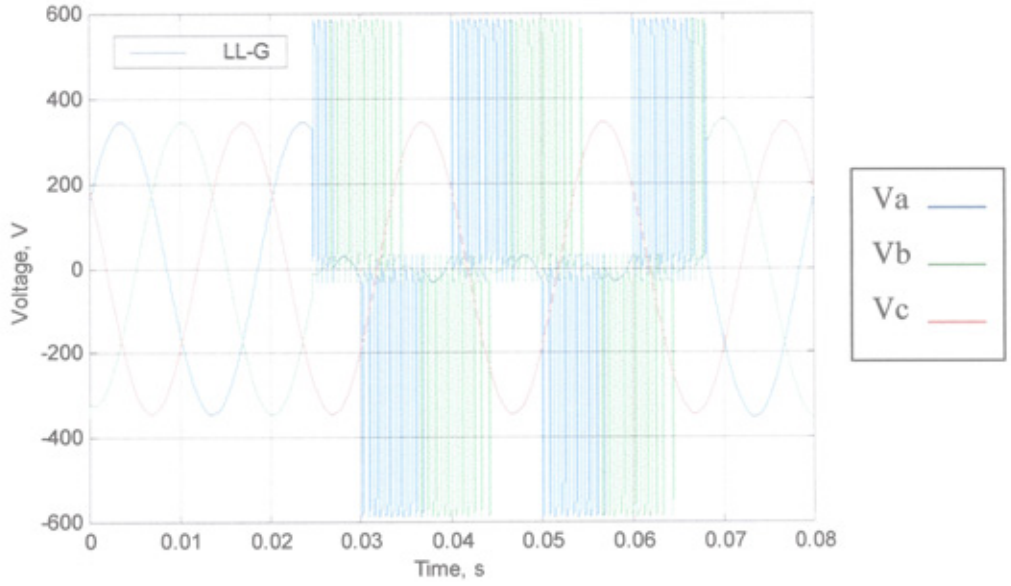


Figure 2.19 Voltage waveforms during a L-L-G fault with FCLID

Line to line fault (two FCLID in operation)

The current and voltage waveforms at the secondary side of the transformer for a line to line fault are shown in Figures 2.20 and 2.21. It is clear from these Figures that only one FCLID operate and the second FCLID continuous conducting since the current through it does not exceed Imax. Also the losses in both IGBTs and varistors are less than the losses in case of other faults (single-line or double line to ground faults).

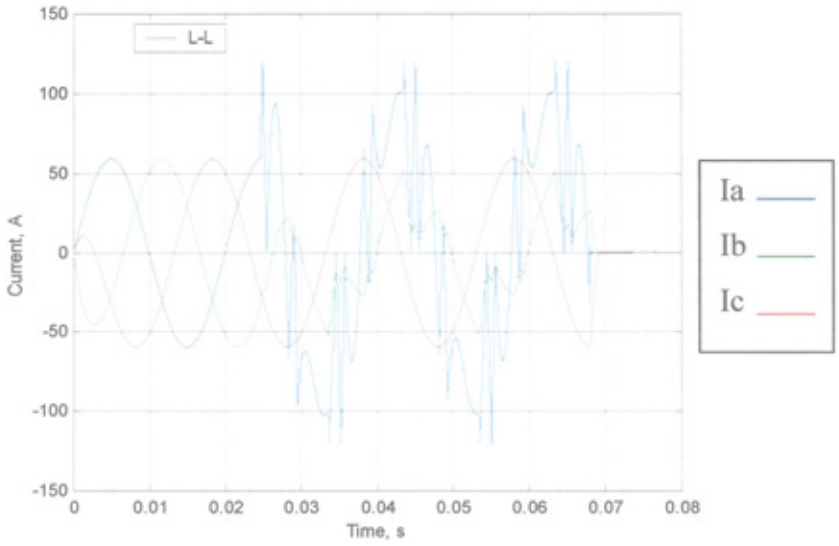


Figure 2.20 Current waveforms during a L-L fault without FCLID

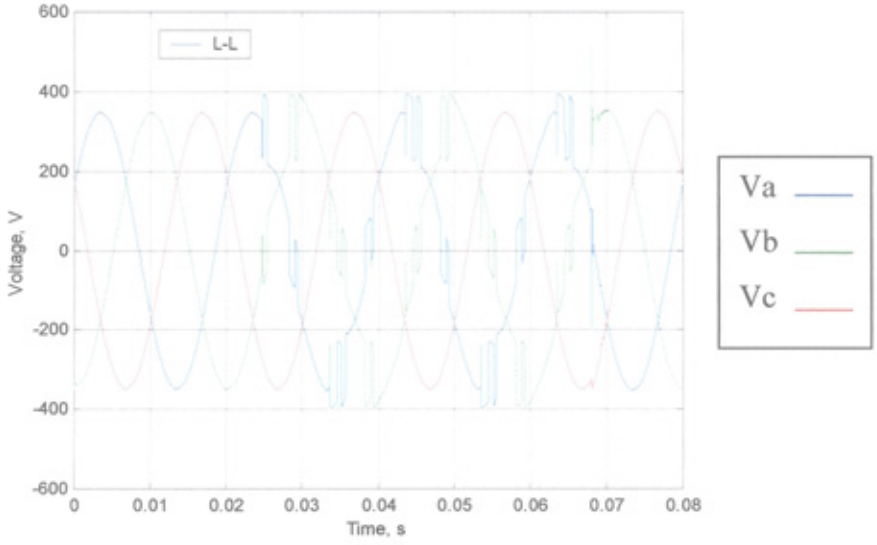


Figure 2.21 Voltage waveforms during a L-L fault without FCLID

Line to line fault (one FCLID in operation)

In case of line-to-line fault, it is possible to interrupt one FCLID completely and let the other FCLID supply the load of both phases. The current and voltage waveforms at the secondary side of the transformer for a line to line fault are shown in Figures 2.22 and 2.23. It is clear from the simulation results on the three-phase system that the FCLID can operate effectively for all types of three-phase faults.

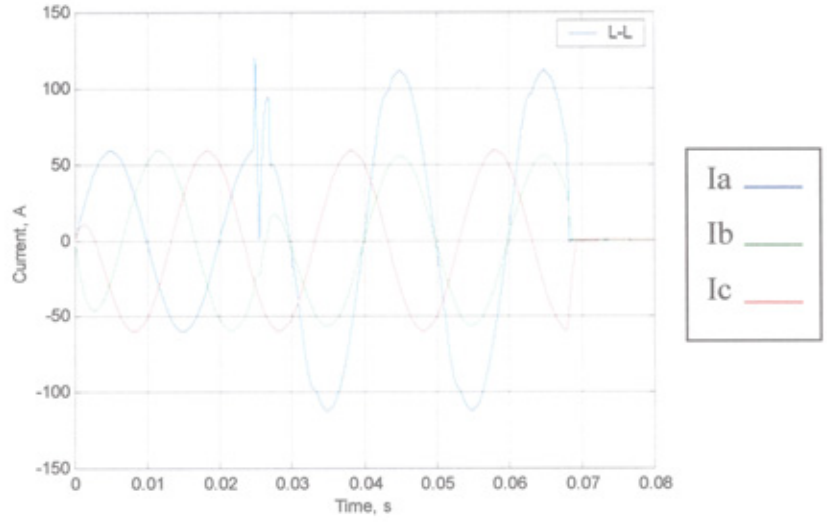


Figure 2.22 Current waveforms during a L-L fault without FCLID

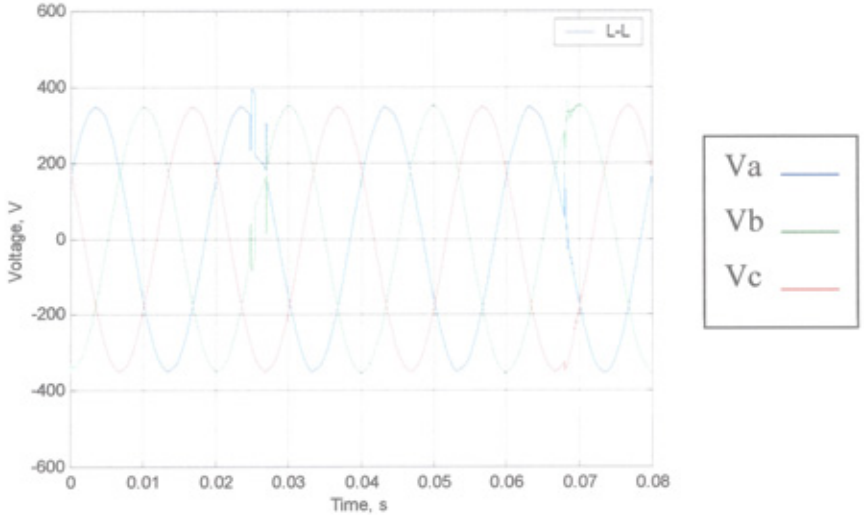


Figure 2.23 Voltage waveforms during a L-L fault without FCLID

2.7 Effects of The FCLID on The Quality of Supply

Power supply quality enhancement is a very important issue for both utilities and customers because of the extensive use of sensitive loads. Among the various types of disturbances affecting voltage quality (e.g. surges, harmonics, spikes, etc.), the most serious impediments are voltage sags. Voltage sags and their associated phase-angle jumps may cause equipment malfunction or damage which leads to production stop with associated costs; these costs include production losses, equipment restarting and damages [31,32]. A common cause of voltage sags is short-circuit faults [33,34]. When a fault occurs in a distribution network, a voltage dip appears on all the affected busbars in the network. The level of the voltage dip depends on the point of common coupling and the electrical distance of the bus from the fault. Utilities and large customers are both interested in cost-effective sag mitigation techniques. Many power electronics based devices have been developed for sag mitigation such as; Distribution Static Compensator (D-STATCOM), Dynamic Voltage Restorer (DVR), Thyristor Controlled Series Capacitor (TCSC), Static Transfer Solid-state Switch (STSSS) and Solid-state Fault Current Limiter (SSFCL) [35-40]. Some of them have the disadvantage of high cost and other cannot limit the fault current to less than 5 times of the normal current. The following sections explain the voltage sag, and examine the performance of the FCLID on the network operations and how it could be used to mitigate voltage sags.

2.7.1 Voltage sag

Voltage sag is a reduction in the r.m.s. value of the voltage (0.1 p.u.- 0.9 p.u.) for a duration between half a cycle and several seconds. Power quality surveys reveal that

80 % to 90% of customer's complaints are due to voltage sags. Most of these are due to short circuits faults in the power system. [41].

The voltage sag magnitude (i.e. the voltage during the sag) for a fault somewhere in a radial distribution system depends on the point of common coupling (PCC). Figure (2.24) gives the equivalent circuit of a radial power system shown in Figure (2.4): Z1 is the source impedance at the PCC; Z2 is the impedance between the PCC and the fault (including any fault impedance). The voltage magnitude (in p.u.) at the PCC (neglecting the effect of the load) is:

$$V = \frac{Z_2}{Z_1 + Z_2}$$

It should be noted that this voltage can change depends on the PCC, network configuration and the fault location.

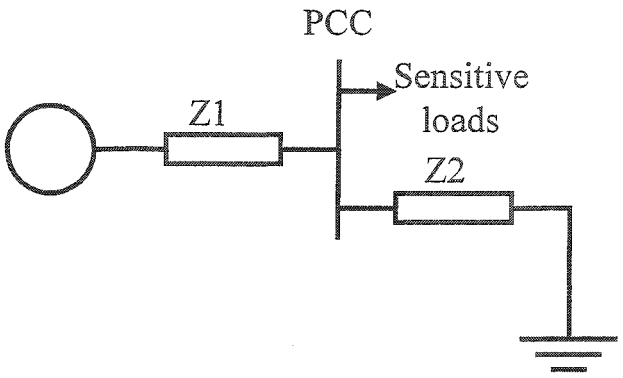


Figure 2.24 A simplified model of a power system

To explain the effects of the FCLID on voltage sag, a single-phase to ground fault at different locations (close to the FCLID and at the end of the cable) of the network shown in Figure (2.4) is simulated. Figure (2.25) shows the Voltage r.m.s value for a system without FCLID. The fault is initiated at .01 s and cleared at .07 s. Figure (2.26) shows that the FCLID reduced the voltage sag to 3 % or less. The FCLID can mitigate voltage

sags without increasing the short-circuit level as compared with other voltage sag mitigation devices. In case of a permanent fault the FCLID is capable to interrupt the fault current at any desired instant, isolating the faulty feeder only. Therefore, this device will help in minimising the number of interruptions and preventing loose of supply for the unfaulty feeders.

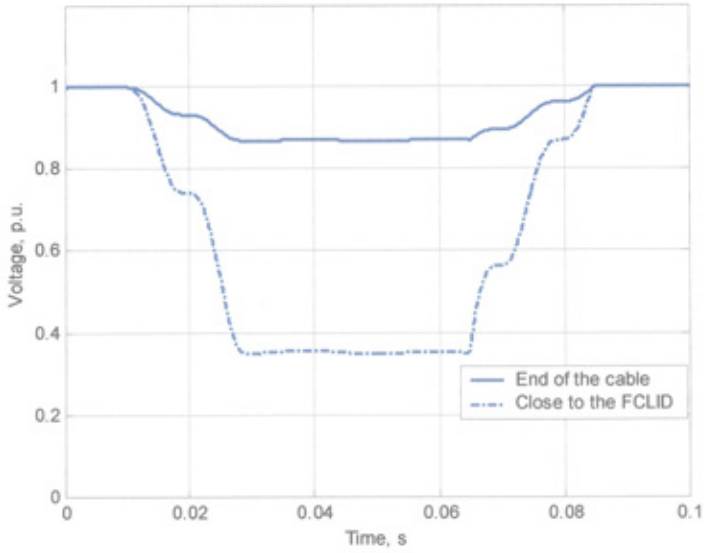


Figure 2.25 Voltage profile (r.m.s.) for a system without FCLID

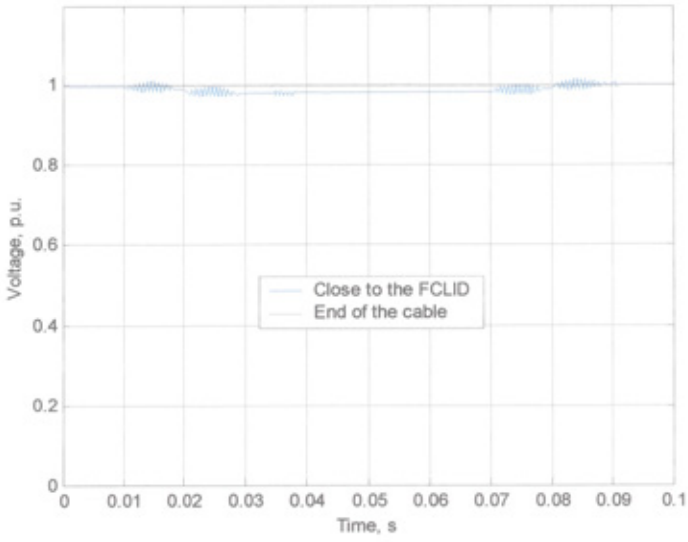


Figure 2.26 Voltage profile (r.m.s.) for a system with FCLID

2.7.2 Phase angle jump

A short circuit in a power system not only causes a drop in voltage magnitude but also a change in the phase angle of the voltage. The phase angle jump manifests itself as a shift in zero crossing of the instantaneous voltage. A phase angle jump is not a problem for most equipment. But power electronics converters using phase angle information for their firing instants may be affected. The phase angle jump may cause problems for drive systems, such as speed change, misfiring and commutation failure [41]. Also a phase angle jump can upset the operation of ASVCs, reduce their voltage sag mitigation effect and cause high post-sag overvoltage [42]. The study on the operation of the a.c. contactor shows that not only the voltage sag magnitude and duration affect the operation of the contactor but also the phase angle jumps [43].

The effect of the FCLID on the phase angle jump during a single-line to ground fault have been investigated. Figures 2.27 and 2.28 show the three phase line-to-line voltages and corresponding phase angles for a short-circuit which results in a fault current of 3 kA. The voltage sag is about 20 % and the phase angle jumps from 60° to 69° for Vab and from 180° to 171°for Vca. Figures 2.29, 2.30 and 2.31 show the current, voltage and phase angle when the FCLID is installed in the network. It can be seen that the FCLID not only improves the voltage sag but also prevent phase angle jumping, keeping the system balanced.

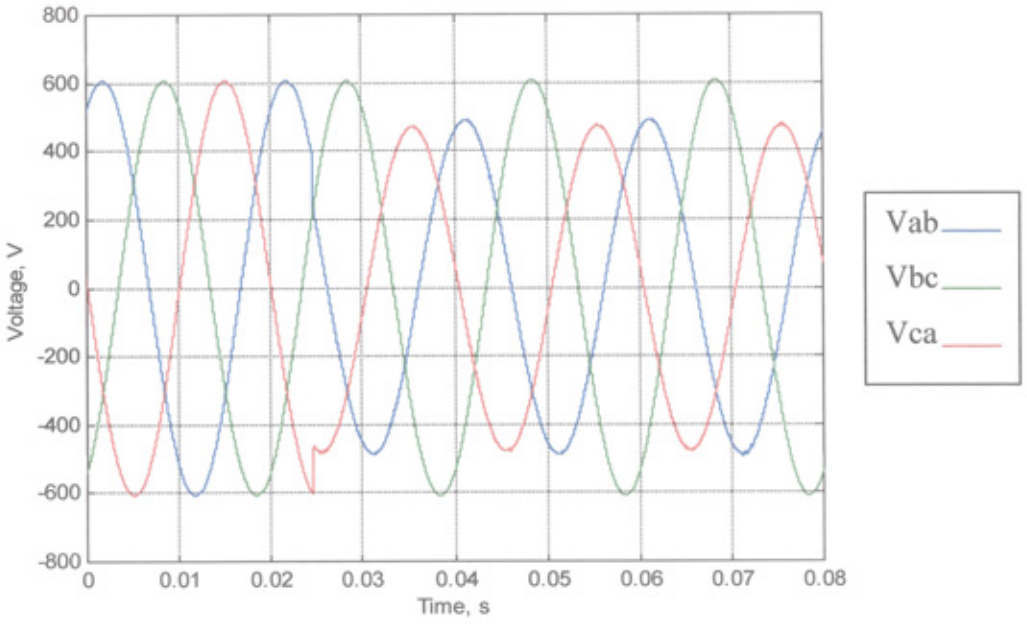


Figure 2.27 Three-phase voltage waveforms (without FCLID)

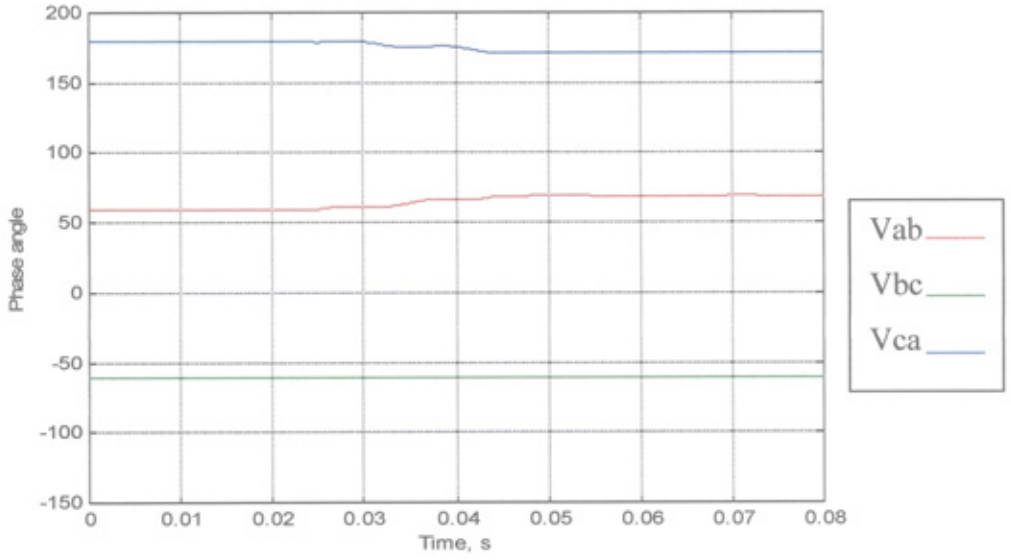


Figure 2.28 Phase angles (without FCLID)

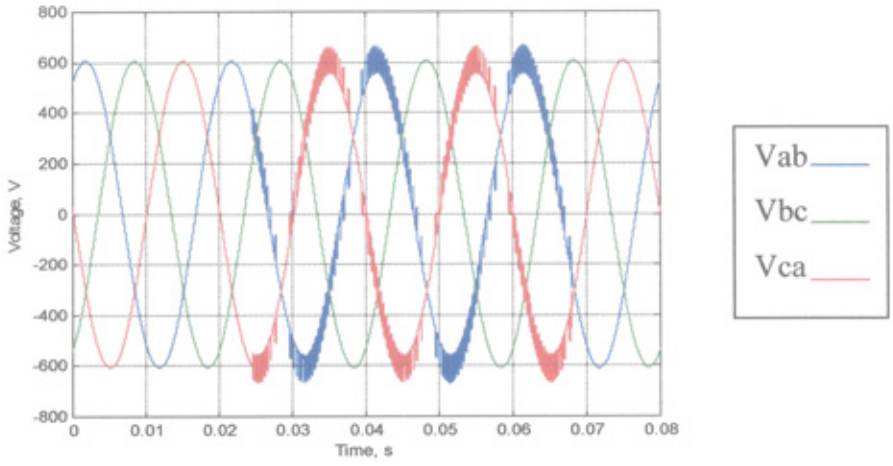


Figure 2.29 Three-phase voltage waveforms (with FCLID)

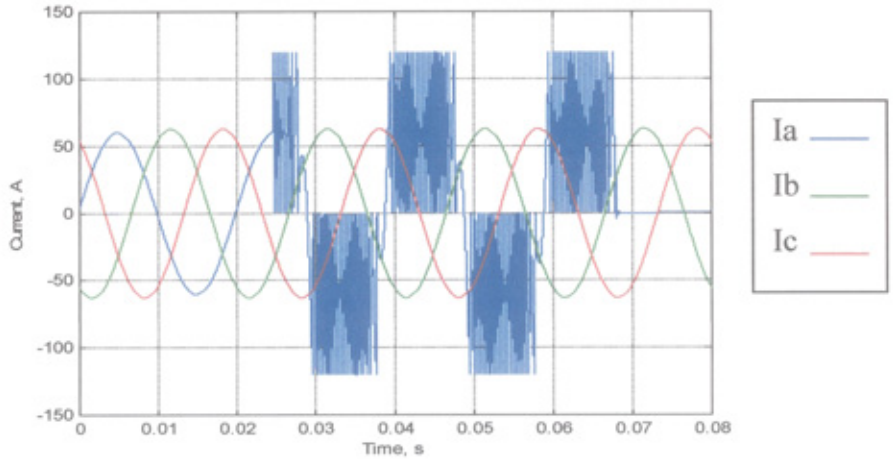


Figure 2.30 Three-phase current waveforms (with FCLID)

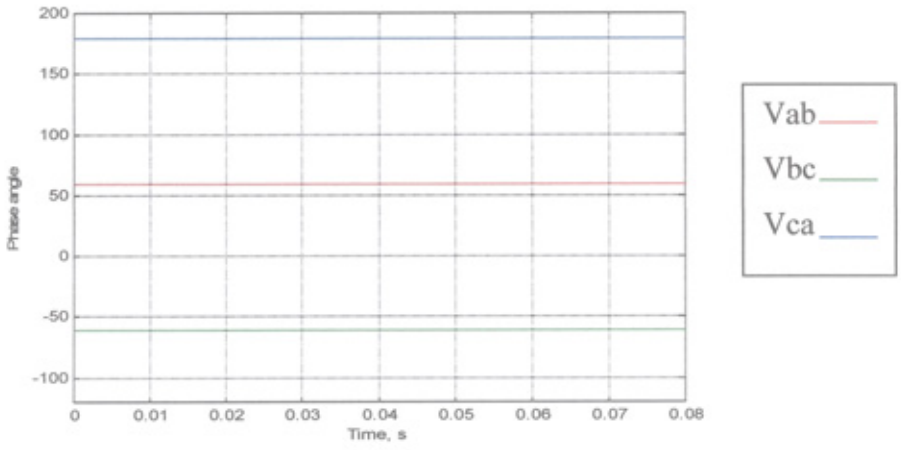


Figure 2.31 Phase angles (with FCLID)

2.8 Conclusions

In this chapter a simulation model of the FCLID, developed using MATLAB/SIMULINK and POWER SYSTEM Blockset, has been described. The performance of the proposed FCLID in a typical distribution network of NEDL is also given. The results obtained show that:

- The FCLID is able to limit the short circuit current to a safe level for a period determined by the FCLID component ratings (IGBT and Varistors).
- The proposed FCLID can operate well for all types of fault in a three-phase system. In the case of a line to line fault, the losses of the device are less than in the other cases (single line-to-ground or double line-to-ground faults). Also it is possible to interrupt the FCLID in one phase and let the other FCLID supply the loads on both phases. So it is recommended to differentiate between different types of faults to define the FCLID operation mode.
- The performed analysis (refer to Figures 2.25 and 2.26) demonstrates the FCLID effectiveness in mitigating voltage sags caused by short circuit faults at different locations.
- The operation of the FCLID improves the system unbalance during a single-line-to-ground fault by reducing the phase angle jump.
- Installation of the FCLID in the distribution network will improve the quality of supply by reducing voltage sag, preventing the unnecessary operation of the protection system; hence minimising the number of interruptions to the unfaulty parts.

CHAPTER THREE

SOLID-STATE SWITCHES FOR THE FCLID

3.1 Introduction

The semiconductor switch is the main building block of the FCLID. The revolution in power electronics has resulted in cost reduction, performance improvement, and widespread application of semiconductor devices. The evolution of power semiconductor devices and their associated technology started with the invention of the bipolar transistor in the late 1940s and the thyristor in 1956 [44]. Since then, many power semiconductor devices have been produced such as the triac and the gate-turn-off (GTO) thyristor. Recent technical advantages have resulted in the evolution of conductivity modulated MOS devices such as the insulated gate bipolar transistors (IGBT), MOS-controlled thyristors (MCT), integrated gate commutated thyristors (IGCT) and emitter turn off thyristors (ETO). These devices offer some improved characteristics compared with earlier conventional silicon devices [45]. The technological advances in controllable power semiconductor devices (capable to turn off by a control signal) makes the development of the FCLID for distribution networks possible.

IN THIS CHAPTER the characteristics of the controllable semiconductor switches are discussed in the view of FCLID application. The requirements of the FCLID and factors affecting the selection of the semiconductor device are described. Techniques for estimation and prediction of junction temperature for semiconductor devices are presented. A method for predicting the IGBT junction temperature to protect the FCLID from damage is proposed and described.

3.2 Selection of The Solid-State Switching Device

The FCLID has set of requirements that must be met by choosing a suitable switching device to make the FCLID capable of delivering the stated performance (limiting and interrupting the fault current safely). The requirements for the solid-state switch are as follows:

1. Rated voltage.
2. Maximum controllable current (maximum pulsating current for IGBT).
3. Turn-on and turn-off time.
4. Switching frequency and loss.
5. Maximum acceptable junction temperature.
6. Wide safe operating area
7. Low transient thermal impedance

Power semiconductor switches suitable for the FCLID, are those that can be turned on or off by applying a gate signal. These devices can be classified as follow:

- Pulse triggered devices such as the GTO, IGCT and ETO [46-48].
- Continuously Triggered devices such as MCT, and IGBT [49,50].

Conventionally for high power applications the gate turn-off (GTO) thyristor has been a dominant choice for a fully controllable semiconductor switch due to its advantages over other devices in terms of current and off-state voltage capability. However, in this application it has been excluded due to its limited switching frequency, high switching losses and the complexity of the gate drive circuit. The IGCT has the advantages of low cost and losses per rated MVA, high reliability and faster switching time than GTO thyristors. After comparison with IGBT the IGCT was excluded due to its low operating

frequency and di/dt constraints. The IGBT has become extremely popular in low and medium voltage applications. With the introduction of the HVIGBT, the IGBT presents a challenge to the dominance of the GTO even in the high power area. Therefore, the IGBT has been chosen for developing the FCLID in this study as it better meets all the requirements of the FCLID (for example, its max. junction temperature is 150 °C. as opposed to 115 °C. for GTO and IGCT). For the FCLID to operate as long as possible, the junction temperature of the IGBT needs to be monitored and maintained within a safe limit.

3.3 Estimation of The IGBT Junction Temperature

The junction temperature of the switch is critical in determining the FCLID operating time. Therefore, monitoring the junction temperature with the safe limit is an essential part of the design process. The availability of accurate information about the IGBT junction temperature is essential for the safe and reliable operation of the FCLID (and other power electronic system). However, it is difficult to obtain the actual junction temperature because it can't be measured directly by a non-invasive method. Different techniques for estimating the junction temperature under steady-state operation have been developed and are as follows:

Conventional method:

In this method the junction temperature is estimated from the temperature of the heat sink using a thermal sensor adhered to that heat sink [51]. The estimation of the junction temperature using the thermal sensor has the following drawbacks:

- Errors in thermodynamic model and its constants.
- Variation of thermodynamic time delay according to set-up position of thermal sensor on heat sink.

- Local heating problem in multiple IGBT's on the case.

Using on-state voltage drop:

In this method the junction temperature is estimated using the characteristic of the IGBT in that the on-state voltage drop is a function of the junction temperature and collector current [52]. The method includes two processes, one is the off line characterisation of the IGBT under test and the other is on-line estimation of the junction temperature based on the characteristic data. The natural operation of the FCLID (collector current changes from zero to Imax during the on-state period causing the on-state voltage drop to change from zero to Vce_{max}) makes it quite difficult to measure the instant at which the collector current reaches Imax. So this method is not suitable for FCLID applications.

Similar method [51] is based on the estimation of the IGBT junction temperature using measurements of IGBT's characteristics under different conditions and thermal resistive model of the actual system (neglecting effect of thermal capacitive). Due to difficulty in getting an algebraic expression for the losses, the experimental tests are performed to measure the turn–on and turn-off waveforms under variation of collector current and junction temperature. A method of searching in look-up tables and calculating the loss with linear approximation is applied. Then the junction temperature is estimated from the measured Vce, collector current and estimated power loss. This method is not suitable for the transient estimation and suffers from the disadvantage that it needs several experimental tests for each device to obtain its characteristics.

Using the change in the emitter-base voltage:

In this method the junction temperature of the power transistor is estimated by measuring the change in the emitter-base voltage [53]. This method combines the electrical method with the numerical simulation of the temperature field on the surface of the device and the measured average temperature can be corrected to the peak junction temperature. This method is very time consuming, needs many measurements to simulate the device characteristics and can't be used for the FCLID application due to the change of the on-state voltage drop even during one pulse.

Using the forward current:

In this method, the instantaneous junction temperature of the device is calculated from expressions of the transient thermal impedance and forward voltage drop [54]. The thermal system transfer function is obtained by taking the Fast Fourier Transform (FFT) for the transient thermal impedance expression. Thus, an expression that relates forward voltage drop to the forward current and the junction temperature is used to feedback the influence of the junction temperature variation on the device forward voltage drop. Then, the power loss is calculated by multiplying the measured forward current by the estimated forward voltage drop. Finally, the instantaneous junction temperature is calculated by taking the inverse FFT for the multiplication of the power loss and thermal system transfer function. This method not suitable for the pulsating current and it is very time consuming.

3.4 Proposed Method for Predicting The Junction Temperature of The IGBT

In this method, the current, voltage and switching frequency are measured and used to calculate the average power loss. Based on the measured frequency the transient thermal

impedances at different periods are estimated and the junction temperature of the IGBT can be predicted before it is actually reached (assuming operating conditions to remain the same). Therefore, the FCLID continues to operate as long as the IGBT junction temperature does not exceed the maximum allowable junction temperature.

3.4.1 Equivalent transient thermal impedance

The transient thermal impedance of a semiconductor switch is an important tool in thermal design of power electronic systems. The use of computers and a variety of software packages enable a simulational approach to thermal design [55]. Such an approach requires an accurate thermal model of the semiconductor switch. Figure (3.1) shows the transient thermal model of the semiconductor switch [56&57]. The transient thermal impedance may be expressed mathematically by the sum of exponential terms:

$$Z_{thj-c}(t) = \sum_{i=1}^{n} R_{thi}(1 - e^{\frac{-t}{\tau_i}}) \tag{3.1}$$

where

R_{thi} is the thermal resistance of the i-th RC pair, K/W

$\tau_i = R_i C_i$ is the time constant of the i-th RC pair in seconds.

The number of the exponential functions required for good representation of the Z_{thj-c} curve depends in general on the device topology. However, it has been shown that four exponential terms are enough to model the Z_{thj-c} sufficiently well [57]. Table (3.1) lists the values of the thermal resistances and time constants extracted from thermal impedance curve (shown in Figure 3.2) obtained from the manufacturer data sheets [58]. Figure (3.2) shows the good agreement between the fitted four exponential terms (obtained from the manufacturer data sheet by dividing into four sections) and the manufacturer data sheet.

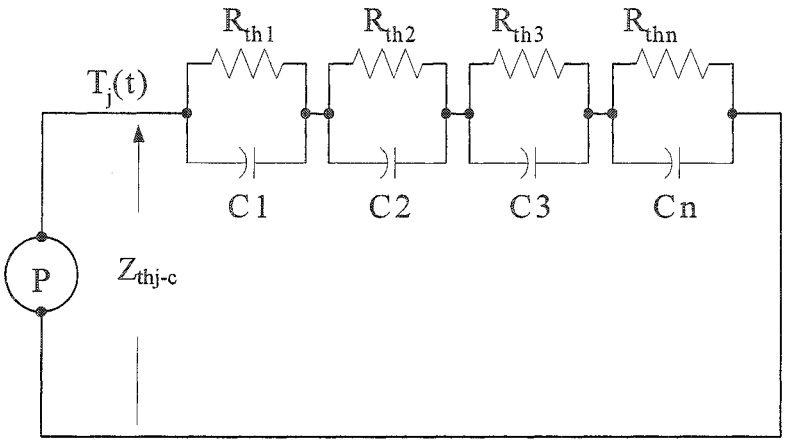


Figure 3.1 Equivalent diagram of the transient thermal impedance

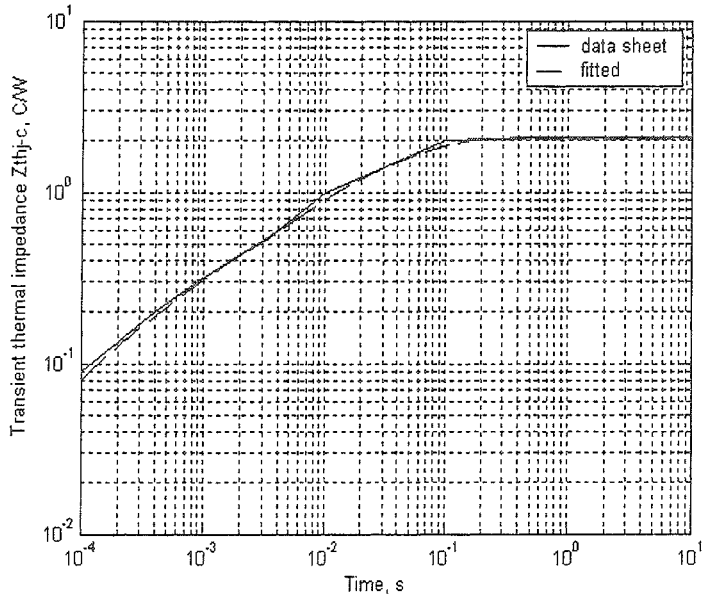


Figure 3.2 Fitted and data sheet Z_{thj-c} curves

No	R_{th}, K/W	τ_i, s
1st	.064	.00009
2nd	.201	.0007
3rd	.7	.0093
4th	1.1	.09

Table 3.1 Thermal model parameters

3.4.2 Junction temperature prediction

The power loss of each switching operation for given current and voltage waveforms of the IGBT is divided into three sections as illustrated in Figure (3.3). The leakage current loss during off state is only a small part of the total loss so that it can be neglected without any significant error [59]. So the total power losses during each pulse of the IGBT are the sum of turn-on, turn-off loss and saturation loss.

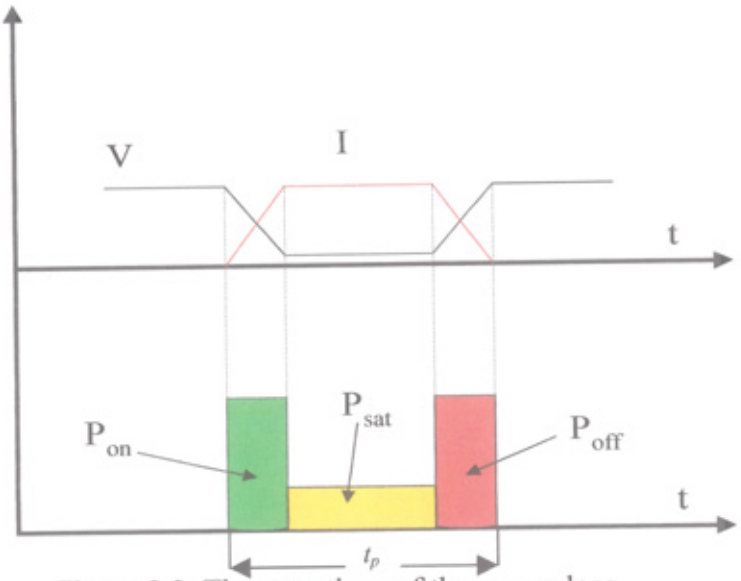


Figure 3.3 Three sections of the power loss

The average power loss for one complete pulse is given by the following equation:

$$P_{av} = \frac{E}{T} = f_s \int_0^{\frac{1}{f_s}} v(t) \times i(t)\, dt \tag{3.2}$$

Where f_s is the switching frequency, $v(t)$ and $i(t)$ are the instantaneous voltage and current over one cycle of period $1/f_s$. Previous research has found that these losses slightly change with a variation of the junction temperature [60]. However, for convenience of analysis, this effect has been neglected. In order to calculate the power losses in the IGBT, the voltage, current and switching frequency are first measured. Then the measured voltage and current are multiplied and integrated over a period T (where T

is greater than the time required to measure the switching frequency). To simplify the junction temperature calculation for all cases, a duty ratio of 50 % for all waveforms is assumed. Figures 3.4 and 3.5 show the actual and normalised power loss waveform. Note that the average power loss in both cases is the same and is equal to the actual total power loss (P_{sat}, P_{on} and P_{off}).

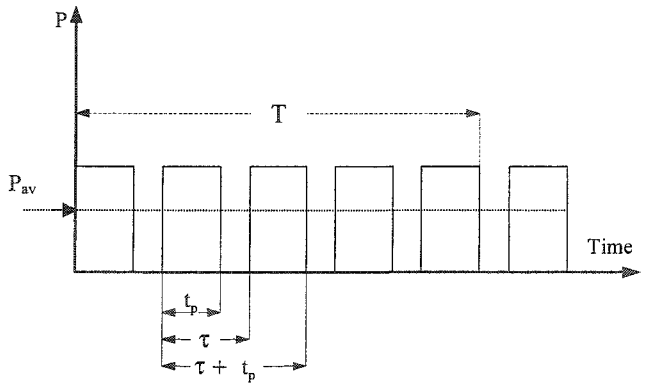


Figure 3.4 Power loss waveform (t_p = pulse width and τ = cycle width)

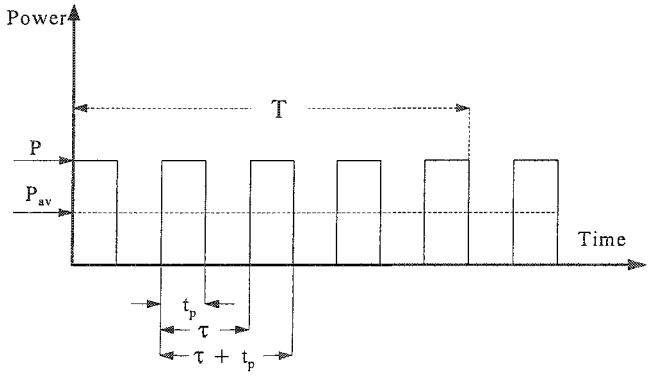


Figure 3.5 Normalised power loss waveform ($t_p = 0.5\ \tau$)

The average power loss over a period of T can be calculated as:

$$P_{av} = \frac{1}{T} \int_0^T v(t) \times i(t)\, dt \tag{3.3}$$

The peak value of the power loss for the normalised pulse is:

$$P = 2 \cdot P_{av} \tag{3.4}$$

The temperature rise at any time during transient condition for continuous repetitive pulses can be calculated by the following equation [57&59]:

$$\Delta T_j = P\left[\frac{t_p}{\tau} Z_{th}(t) + (1-\frac{t_p}{\tau}) \cdot Z_{th}(\tau + t_p) - Z_{th}(\tau) + Z_{th}(t_p)\right] \tag{3.5}$$

$$T_j = \Delta T_j + T_a \tag{3.6}$$

where T_a is the ambient temperature.

A computer program was developed to calculate the average power loss, solve the thermal model and predict the junction temperature. As shown in the flow chart given in Figure (3.6), using the measured data (V, I, f_s, T_a.), the average power loss is calculated over a period T. Then, the transient thermal impedance based on the measured frequency is calculated. Finally, the predicted junction temperature is calculated.

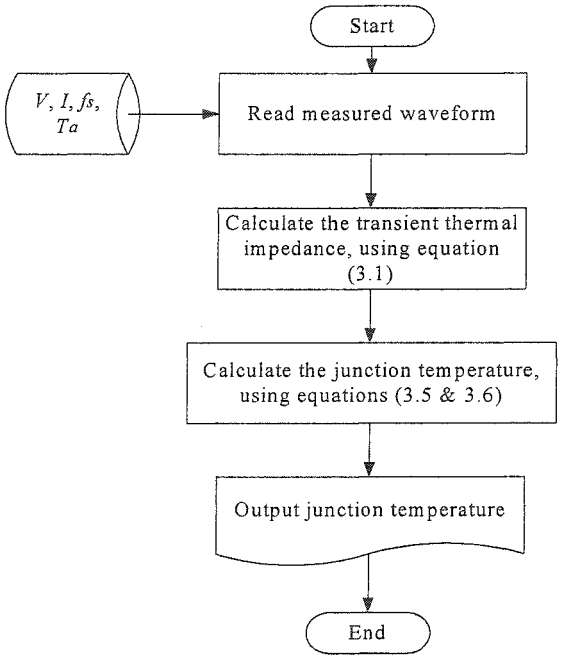


Figure 3.6 Flow chart of the junction temperature prediction

3.4.3 Simulation results

As an example of the temperature prediction, a simple chopper circuit using a single IGBT was modelled in MATLAB/SIMULINK. Figure (3.7) shows a schematic diagram of the simulated circuit. In this diagram two methods are demonstrated. One is the direct method (block B) where the simulated voltage and current of the device are multiplied to calculate the instantaneous power to be fed to the transient thermal impedance model in Figure (3.1). The second method (block A) is the proposed prediction method in which the same current and voltage waveforms as above are used in (3.3), (3.5) and (3.6) to get the average power loss and the predicted temperature at a particular instant. In order to show the effectiveness of this method, three tests have been carried out where the dc voltage = 250 V, load current = 12 A and switching frequency = 240 Hz.. Figure (3.8) shows a comparison between the predicted and actual (this in fact an estimate obtained from the direct method) junction temperature for duty ratios 30 %, 50 % and 70 % respectively.

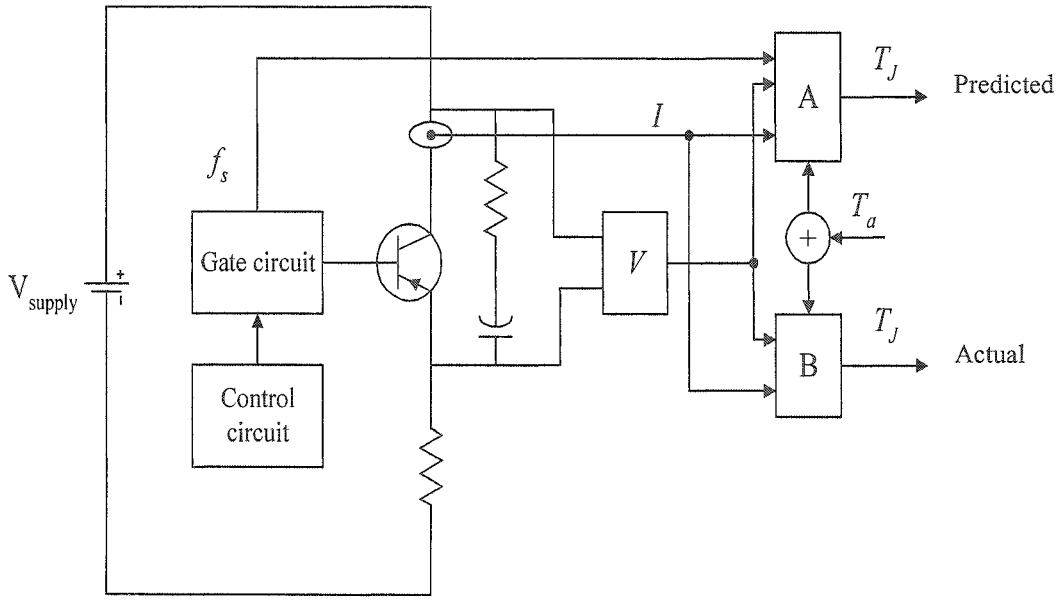
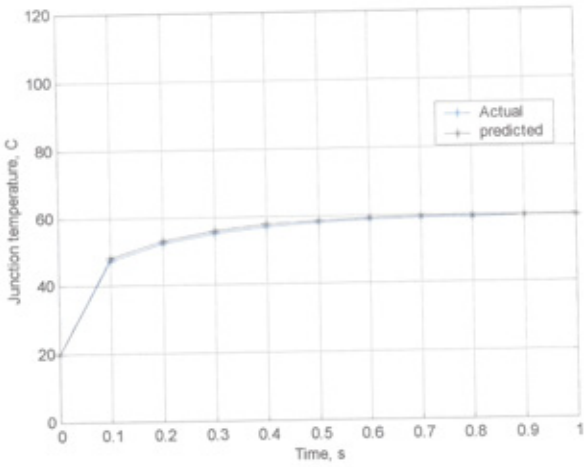
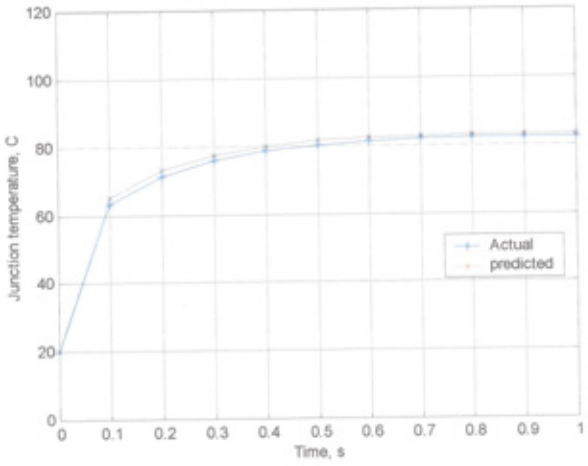


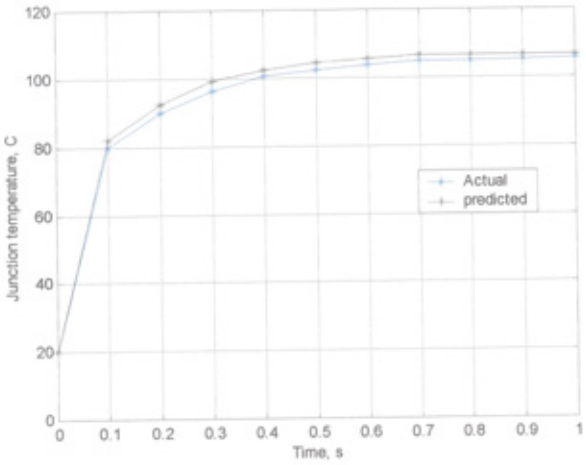
Figure 3.7 Chopper circuit simulation with MATLAB/SIMULINK



(a), D = 30 %



(b), D = 50 %



(c), D = 70 %

Figure 3.8 Comparison between predicted and actual junction temperature

3.4.4 Method validation

In order to verify the simulation results, the test circuit shown in Figure (3.7) has been implemented where the current pulses through the IGBT and switching frequency are set to be of fixed amplitude 12 A and 240 Hz, respectively. Voltage, current waveforms and frequency were recorded into a storage oscilloscope for the sake of temperature prediction and actual temperature determination (as explained in Section 3.4.3) during the operation from a few milliseconds up to a second. Figure (3.9) shows the comparison between the predicted and measured (actual) junction temperature with duty ratio 35 %, 50 % and 65 % respectively.

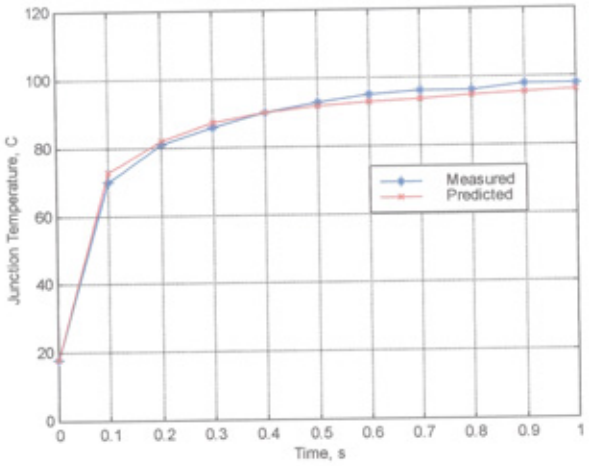
Table (3.2) summarises the results and percentage error. It can be seen that the prediction errors within the 300 ms are in the range ± 7.2 %, then decrease to 3.5 % or occasionally to zero. The accuracy of the proposed method depends up on the accuracy of the measuring devices and on the accurate transient thermal impedance data of the used switch.

3.5 Prediction of The FCLID Operating Time

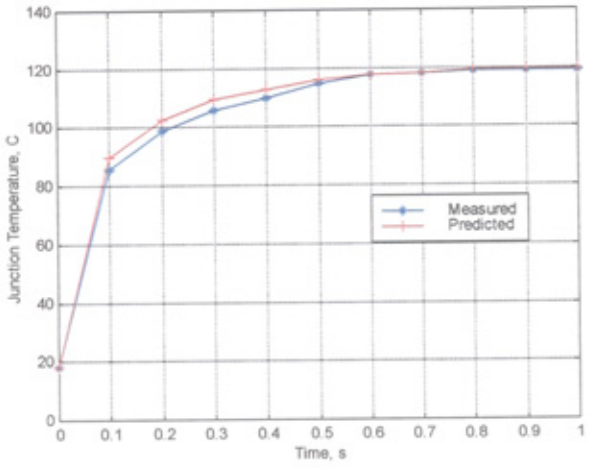
For safe operation of the FCLID the maximum allowable junction temperature of the IGBT is chosen to be 120 °C. The transient thermal impedance $Z_{thj-c}(t)$ can be calculated from Equation (3.5) and expressed as:

$$Z_{thj-c}(t) = 2 \cdot [\frac{\Delta T_j}{p} - ((1 - \frac{t_p}{\tau}) Z_{th}(\tau + t_p) - Z_{th}(\tau) + Z_{th}(t_p))] \tag{3.7}$$

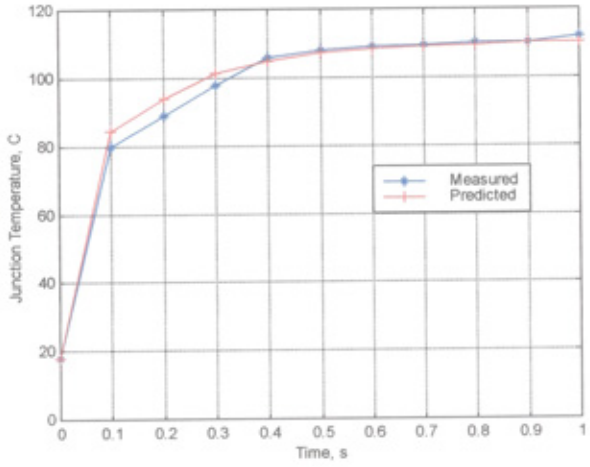
To simplify the analysis, only one exponential term of the transient thermal impedance (Equation 3.8) is used. This approximation is fairly accurate as shown in Figure (3.10).



(a), D = 35 %



(b), D = 50 %



(c), D = 65 %

Figure 3.9 Comparison between predicted and measured junction temperature

	Duty ratio 35 %			Duty ratio 50 %			Duty ratio 65 %		
Time, s	T_m, C	T_m, C	Error %	T_m, C	T_p, C	Error %	T_m, C	T_p, C	Error %
0	18	18	0	18	18	0	18	18	0
.1	52	55	5.76	62	66.5	7.2	68	72	5.8
.2	63	64	1.58	71	76	7	81	84.5	4.3
.3	68	69.1	1.6	80	83.3	4.12	88	91.5	3.9
.4	72	72	0	88	87	-1.13	92	95	3.2
.5	75	74	-1.3	90	89.2	-0.89	97	98	1.03
.6	77	75	-2.59	91	90.5	-0.54	100	100	0
.7	78	75.5	-3.2	91.4	91.2	-0.22	100.2	100.4	0.19
.8	78	76.8	-1.53	92	91.5	-1.6	101.2	101.4	0.19
.9	80	77.2	-3.5	92	92	0	101.2	101.4	0.19
1	80	78	-2.5	94	92	-2.1	101.2	101.4	0.19

Table 3.2 Comparisons between predicted and measured junction temperature

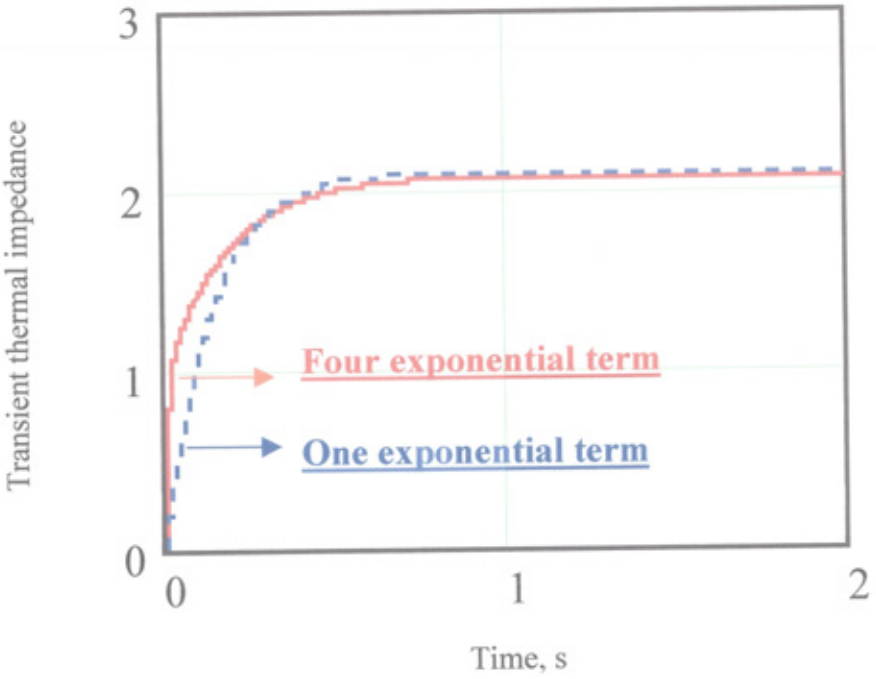


Figure 3.10 Comparison between simplified and actual transient thermal impedance curves

$$Z_{th}(t) = R_{th} \cdot (1 - e^{\frac{t}{\tau}}) \tag{3.8}$$

The FCLID operating time can be expressed as:

$$t = \tau \cdot \ln\left(\frac{R_{th} - Z_{th}(T_J = 120)}{R_{th}}\right) \tag{3.9}$$

In this study the operating time of the FCLID is determined by the varistor energy handling capability as explained in Chapter 4, so the junction temperature of the selected switch is calculated to ensure that the FCLID operate within its safe operating limit. Figure (3.11) shows the IGBT junction temperature under the FCLID operation, the short-circuit level is set to 1 kA. Figure (3.11) illustrates that the junction temperature of the IGBT reaches the steady state after 0.3 s, so the device can operate safely up to 1 s.

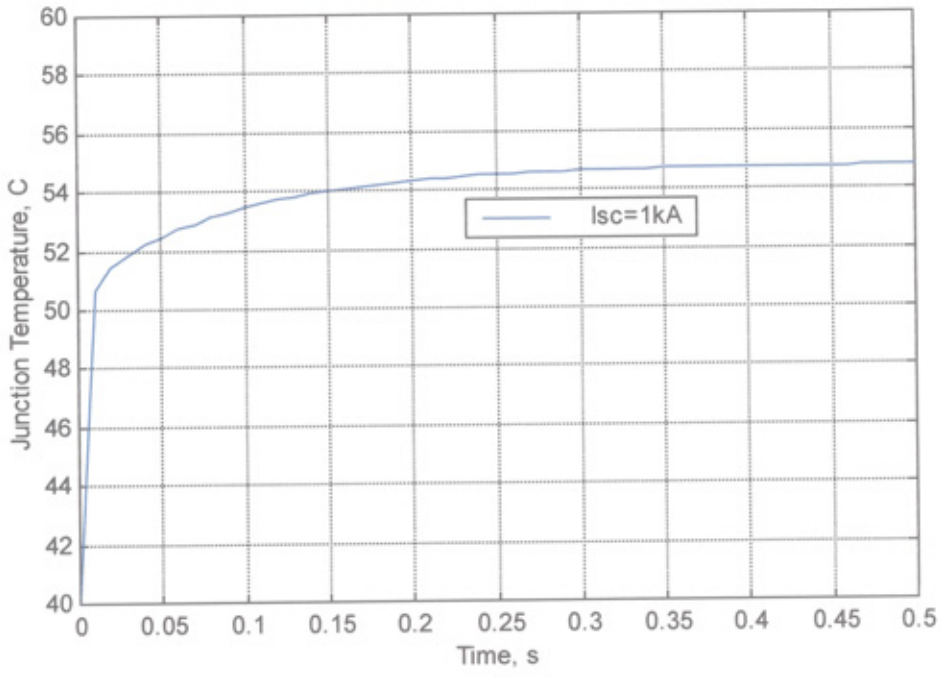


Figure 3.11 Calculated IGBT junction temperature

3.6 Conclusions

This chapter reviewed commercially available power semiconductor switching devices in relation to their suitability as the switching element for the FCLID application. Based on this review, the IGBT has been selected as having the most desirable attributes. It is a voltage-controlled device thus, simplifying the gate drive circuitry. It has a low transient thermal impedance, low switching losses and can operate at high frequency. In addition, the IGBT normally fails as open-circuit which makes the FCLID a fail-safe device.

Several methods have been developed for estimating the junction temperature of the solid-state switch in steady state but not during transient operation. For this reason, a new method for predicting the IGBT junction temperature under transient conditions has been presented and implemented. Apart from this merit, this method has the following important advantages:

- It reduces the time consumption for modelling the device characteristics (forward voltage and power loss).
- It can predict the junction temperature of the semiconductor switch at any instant during transient condition.
- It can prevent damage of the switching devices during transient or fault period by sending a signal to the controller to reduce stress (by decreasing either the current or the switching frequency).

Using this method the maximum operating time of the FCLID can be predicted. It also allows the FCLID controller to change the magnitude of the maximum & minimum current and operating time to suit the specific system requirements.

CHAPTER FOUR

VARISTORS FOR THE FCLID

4.1 Introduction

Metal oxide varistor are ZnO-based ceramic devices having highly non-linear current voltage characteristics similar to those of the back-to-back zener diodes. They are widely used as voltage clamping elements in many applications including solid-state circuit breakers, fault current limiting devices, active filters and other switching power electronic systems. During the FCLID operation the varistor is subjected to repetitive pulses and hence is required to have a high energy handling capability.

THIS CHAPTER gives an overview of the electrical and microstructural properties of ZnO varistors. Also, it provides an overview of failure modes of the varistor and describes the electrical uniformity of the ZnO varistor when repetitive current pulses are applied. Non-destructive tests to evaluate the uniformity of the varistors using a scanning acoustic microscope are also presented. Experimental tests, using an infrared thermal imaging system, to evaluate the energy handling capability of the varistor are also presented. Finally, a new method for improving current sharing between parallel varistors is described.

4.2 Electrical Properties of ZnO Varistors

ZnO varistors have highly non-linear voltage (V) - current (I) characteristics above a threshold voltage. Since the range showing the highly non-linear property is wide, the V-I characteristics are usually expressed logarithmically, as shown in Figure (4.1) [61].

Functionally, the varistor acts as a linear insulator (resistor) prior to reaching a voltage known as the breakdown or threshold voltage, and it act as conductor thereafter. The electrical features that make the ZnO varistor attractive to the designer are the non-linear characteristics in the conductive mode and the low leakage current (power loss) in the resistive mode (steady state operating voltage) [62].

The V-I characteristics of the ZnO are classified into three regions, as shown in Figure (4.1). In the leakage current region, below the threshold voltage (typically a voltage at 1 μA), the non-linear property is not so prominent and highly dependent on the temperature. In normal varistor region, between threshold voltage and a voltage at a current of about 100 A, the non-ohmic property is very prominent and independent of temperature. In upturn region, above 100 A, the non-linear property gradually decays. ZnO varistors are characterised by the magnitude of the non-linear exponent α-values and the width of the range where the highly non-linear property is exhibited. Varistor's definition and terms are presented in APPENDIX B [63].

The varistors used in the FCLID operate in the normal varistor region, due to the high non-linearity in this region it is difficult to match the varistor characteristics connected in parallel to achieve the FCLID energy rating. This problem is discussed in section (4.9).

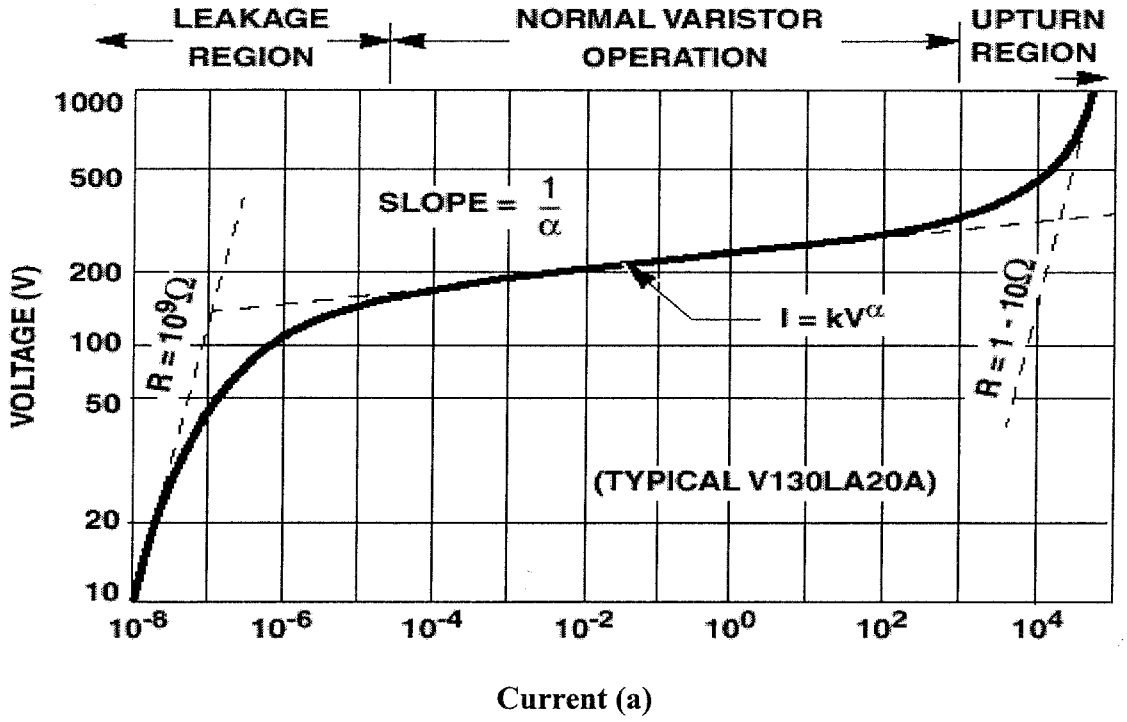


Figure 4.1 V-I characteristics of ZnO varistor [62]

4.3 Varistor Microstructure

Figure (4.2) shows an idealised representation of the microstructure of the ZnO varistor [64]. The ZnO grains, of an average size d, are completely surrounded by an insulating oxide of thickness t. Each ZnO grain of the ceramic acts as if it has a semiconductor junction at the grain boundary. Since the non-linear electric behaviour occurs at the boundary of each ZnO grain, the varistor can be considered as a "multi-junction" device composed of many series and parallel connection of grain boundaries. The nominal varistor voltage depends basically on the thickness of the device which has a number of grains "n" in series between electrodes. The barrier voltage is normally 2-3 V per grain boundary and does not vary for grains of different sizes. Hence, mean grain size and grains distribution plays a major role in electric characteristics of the varistor. For this

reason smaller grain sizes with uniform distribution are always desirable for the performance of the varistors [64].

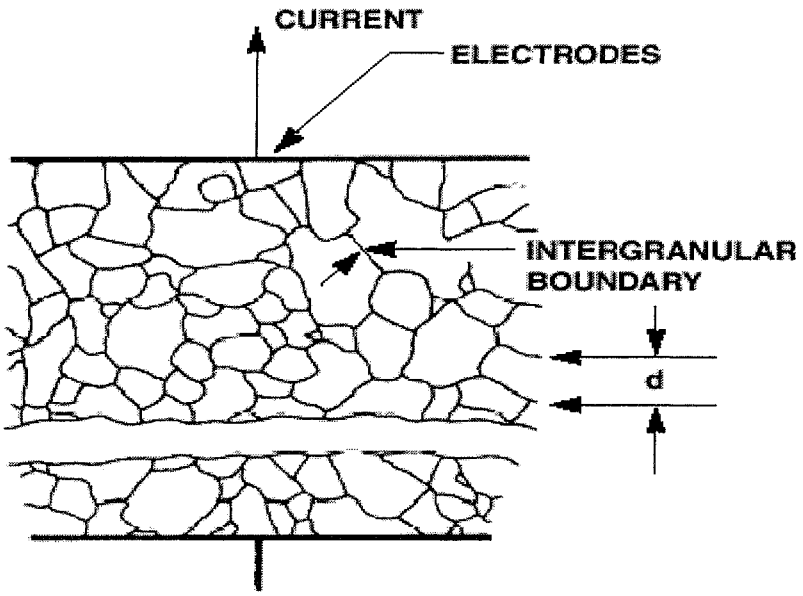


Figure 4.2 Idealized microstructure of the varistor

Figure (4.3) shows a back-scattered secondary electron image obtained for a varistor specimen. The micrograph clearly shows that there are three phases (i) grains, (ii) integranular material and (iii) particles. The actual microstructure is thus considerably more complex than the idealised representation. The ZnO grains are the dominant phase in the varistor microstructure. The intergranular material is the white area surrounding the ZnO grains. This area corresponding to a phase which may be bismuth oxide rich pyrochlore, $Zn2Bi_3Sb_3O_{14}$. The thickness of this layer acts as an insulating barrier. An increase of this thickness results in an increase in breakdown voltage as illustrated by Emtage [65]. The third phase, represent the particles, are the greyish regions in the micrograph. These particles which may be spinel type structure $Zn_7Sb_2O_{12}$, are insulating and play a second role in determining device properties.

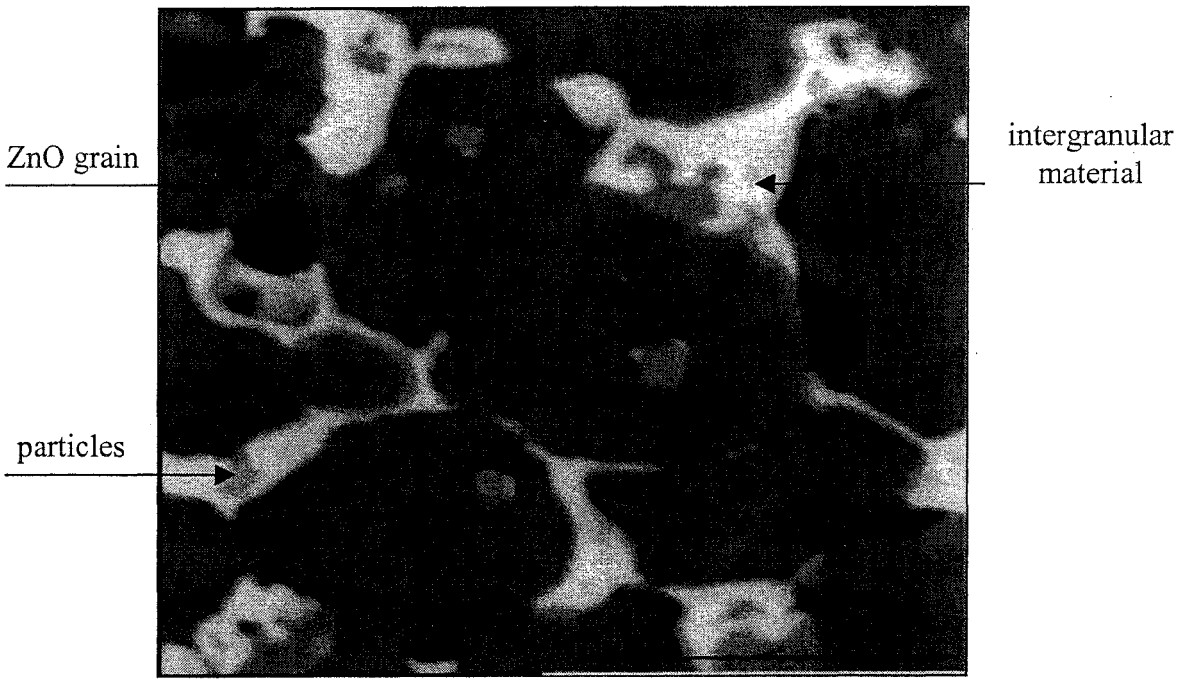


Figure 4.3 Back-scattered secondary electron image of a typical section of ZnO varistor

4.4 Selection of The Varistor

The primary function of the metal oxide varistor is to protect electronic devices and electrical circuits against voltage surges, such as those generated by lighting strikes and circuit switching transients. As varistors are not manufactured for continuous power dissipation, it is appropriate to define the specification of the varistor needed for the FCLID application. The selection of the varistor for the FCLID is a three-step process:

1. Determine the necessary steady-state voltage profile during FCLID operation (varistor nominal voltage should be higher than the supply voltage to prevent excessive leakage current during normal operation of the FCLID (no fault)).
2. Select a varistor rating to provide the required voltage clamping characteristic (clamping voltage should be select carefully, higher clamping voltage the higher stress on the equipment connected to PCC and the lower clamping voltage the higher stress on the varistors).

3. Evaluate and satisfy the energy absorption requirement of the varistor during the FCLID operation.

In the FCLID, the varistor share the current with the IGBT, so it must dissipate continuous energy higher than its rating. The energy handling capability of the varistor is defined as the amount of energy that the varistor can absorb without any failure or damage. In order for the varistor to operate safely, it should be able to absorb this quantity of energy before its temperature rises to a damaging level. In practice, their energy handling capability is limited by one of several types of failure: puncture failure, pulse-induced fracture, and long-term degradation in electrical properties [66]. While the mode of the long-term degradation have been extensively studied and reported [67], there has been a few studies of the two short-term, pulse induced fracture first being described in literature by Eda [68]. The cracking of the varistor is believed to occur when it is subjected to an extremely short pulse. According to Eda [68], the fracture failure mode occurs at short pulses and puncture mode at slightly longer pulses. The puncture failure is believed to occur as a consequence of current localisation and associated Joule heating that lead to a hole being melted in through the varistor and shorting the electrodes. Current localisation can occurs as a result of a variety of geometrical effects, such as electrodes reaching the edge of the sample and shorting down the sides of the varistor. More recently, the possibility of microstructural inhomgeneities, such as variation in the grain boundary potential and grain size, causing current localisation has been explored by computer simulation modelling [69]. The puncture mode of failure is commonly associated with thermal runaway occurring as a consequence of current localisation in the dielectric or semiconductor. The simulation work by Eda [69] reveals that almost any

microstructural variation in properties leads to current localisation and that localisation becomes stronger in the non-linear region. In the FCLID the varistors are subjected to continuous repetitive pulses, which may lead the varistor to fail (puncture mode), for this reason this mode of failure is discussed in section (4.8).

In this research the microstructure uniformity of ZnO varistors are assessed, using three methods which are available:

1. Scanning Electron Microscope SEM
2. Thermal Imaging System
3. Acoustic Scanning Microscope

Varistors tested:

Samples of varistors from three manufacturers were used for this investigation. A 36 mm (sample 1) varistor, 40 mm (sample 2) and a 53 mm (sample 3) varistor. The specifications of the varistors tested are listed in the Table (4.1).

Samples	Sample 1	Sample 2	Sample 3
Diameter	36 mm	40 mm	53 mm
Thickness	2 mm	2.7 mm	3.56 mm
Clamping voltage	560 V	650 V	620 V
Maximum Energy absorption per pulse	170 J	370 J	880 J

Table 4.1 Specification of the Varistors tested

4.5 Microstructural Analysis of ZnO Using SEM

The microstructure of the three samples were analysed by SEM. The secondary electron image (SEI) and back-scattered electron image (BEI) of samples 1, 2 and 3 are shown in

Figures 4.4, 4.5 and 4.6. Sample topography is clearly indicated where as contrast is provided by relating atomic number in BSI.

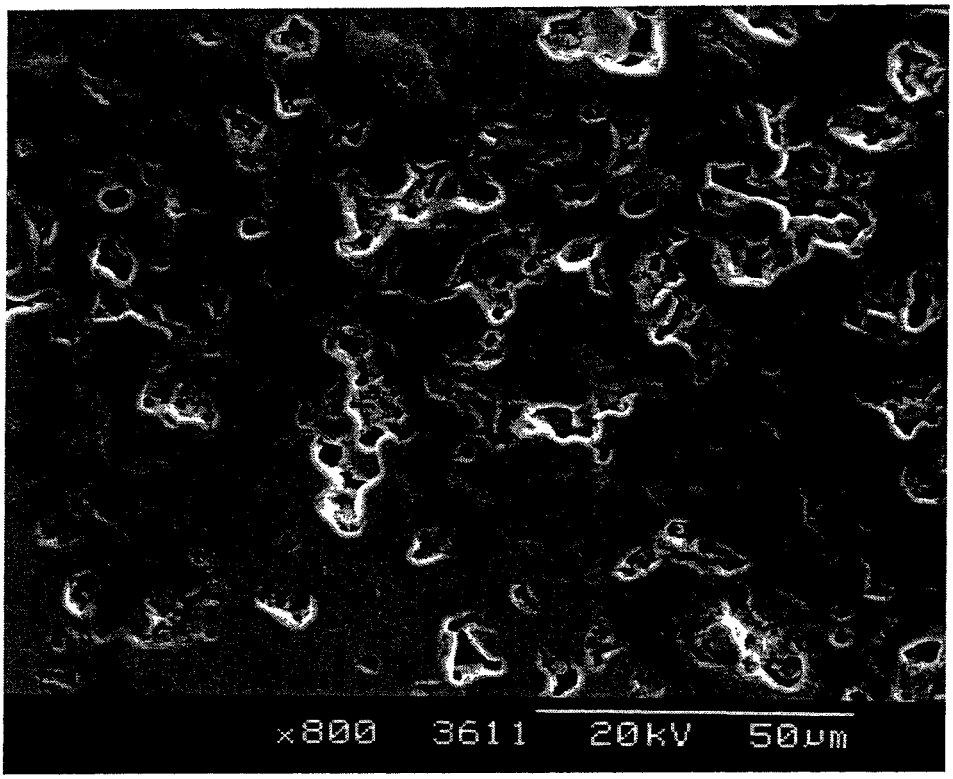
The Four basic compounds formed are ZnO, spinel, pyrochlore and several bismuth rich phases. The location of spinel and pyrochlore is the intergranular phase between ZnO grains. Bi-rich phases exist mainly at the triple point.

In Figure (4.4) the mean grain size of the varistor is 6.06 μm. porosity content is high and other phases are visible. These phases are not distributed well between zinc oxide grains. In Figure (4.5) the mean grain size is 5.95 μm. The porosity contents is high. It can be seen that all phases including the porosity are distributed well. In Figure (4.6) the mean grain size is 6.56 μm. It can be seen that the porosity content is low and all phases are distributed more uniformly.

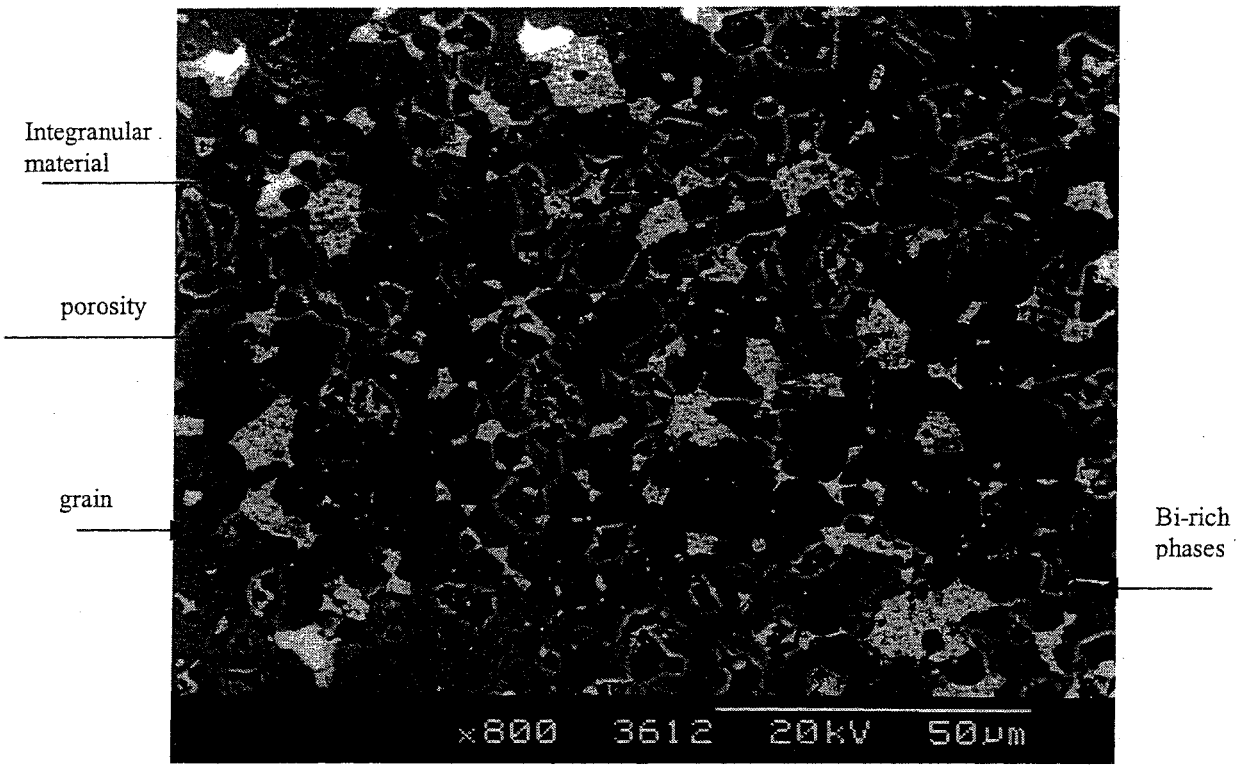
In comparison of the samples 1, 2 and 3, it may be concluded that sample 1 is a poor quality device due to the high porosity content and the distribution of all phases not being uniform. The distribution of all phases for the other samples is uniform with a high porosity content for sample 2.

The results obtained from X-ray energy spectra for each sample are presented in Figures 4.7, 4.8 and 4.9. Due to the high proportion of ZnO in the varistor composition, the spectra are dominated by the ZnO peaks. Smaller peaks for the other phases have been also identified. Comparing these spectra, it is clear that there is a little elemental difference in the constituents used in manufacturing these varistors.

It is suggested that for reliable energy absorption capability the varistor should exhibit all the phases are well distributed with minimal porosity which must also be evenly distributed [70].

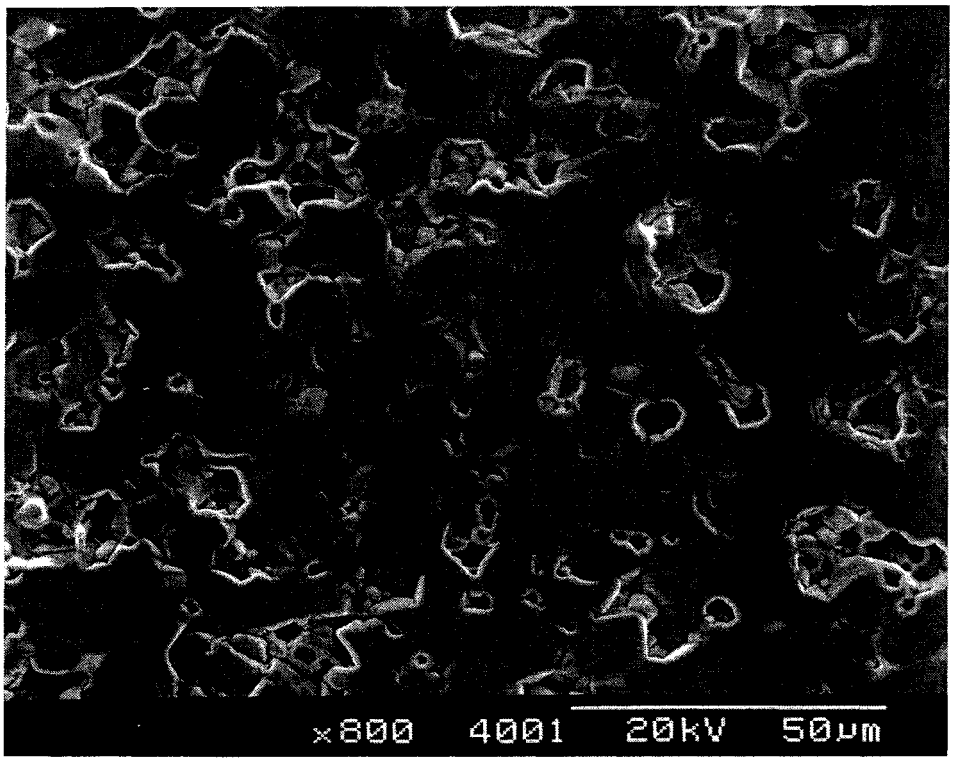


(a) Second electron

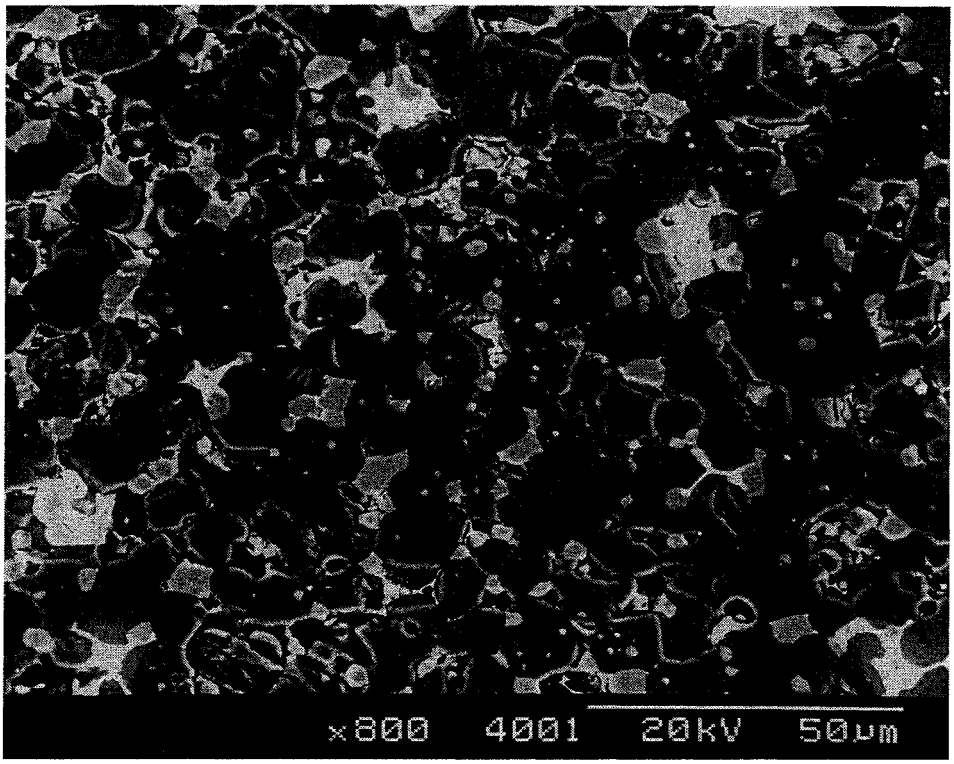


(b) Back scattered electron

Figure 4.4 Micrograph of sample 1

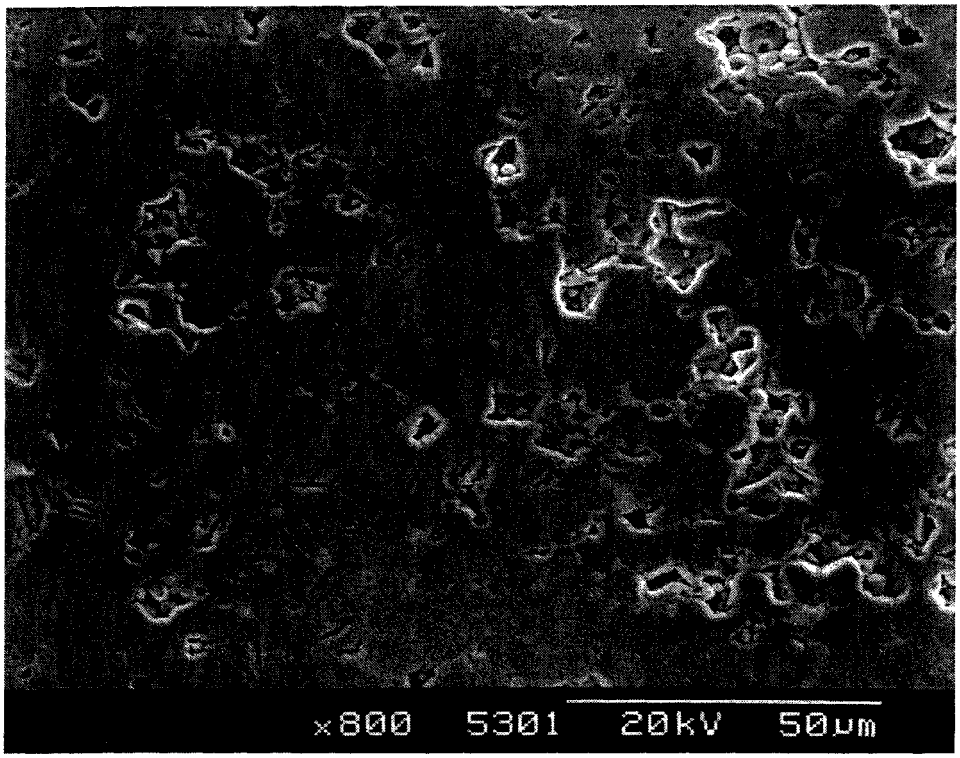


(a) Second electron

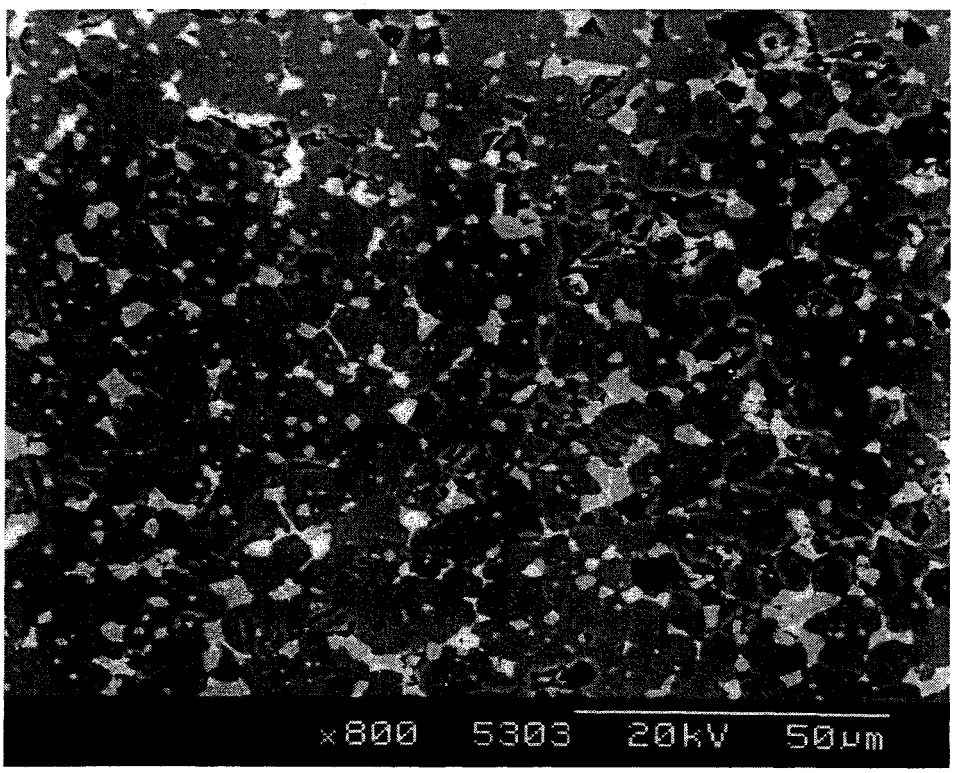


(b) Back scattered electron

Figure 4.5 Micrograph of sample 2



(a) Second electron



(b) Back-scattered electron

Figure 4.6 Micrograph of sample 3

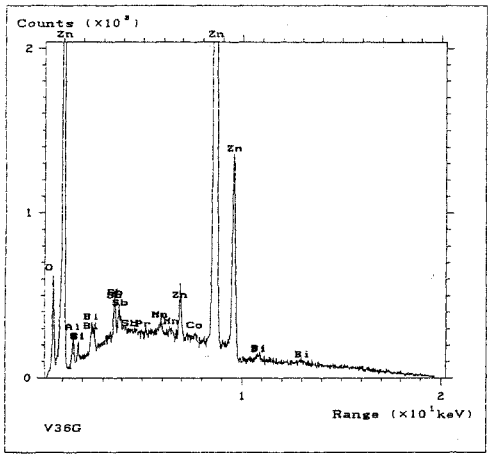


Figure 4.7 X-ray diffraction spectra of sample 1

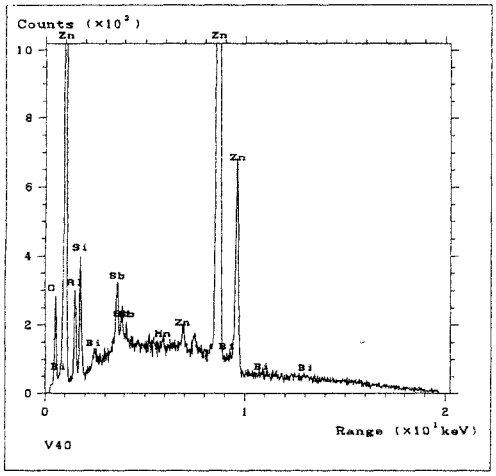


Figure 4.8 X-ray diffraction spectra of sample 2

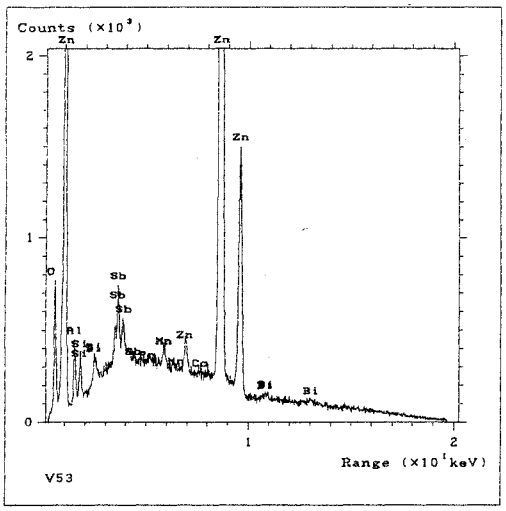


Figure 4.9 X-ray diffraction spectra of sample 3

4.6 Microstructure Uniformity Analysis of ZnO Varistor Using Thermal Image Analysis:

The reason for this test is to find a relationship with the results obtained from SEM. As the response time of most thermocouples will exceed that of the imaging system, they can not be used for measuring the temperature distribution of the varistors. Therefore, an infrared imaging camera was used to measure the temperature distribution of the varistor.

A thermal imaging system has been used in this experiment to interpret the microstructural uniformity by examining the temperature distribution of the Varistor during operation. The specifications of the thermal imaging system are listed in Table (4.2) [71]. The thermal imager allows the user to define the temperature range by adjusting the window and offset. In this test the window 6L and offset 46 were selected to monitor the varistor temperature (see Figure 4.14).

Feature	Specification
Temperature range	-20 to 1500 black body temperature
Focusing range	0.11 m to infinity
Frame frequency	25 Hz
Field of view	16° x 16°
Correction factors	emissivity

Table 4.2 Specifications of the thermal imaging system [71]

Testing the uniformity of ZnO varistors

Figure (4.10) shows a schematic arrangement of the experimental system used in this test and Figure (4.11) shows the experimental set up.

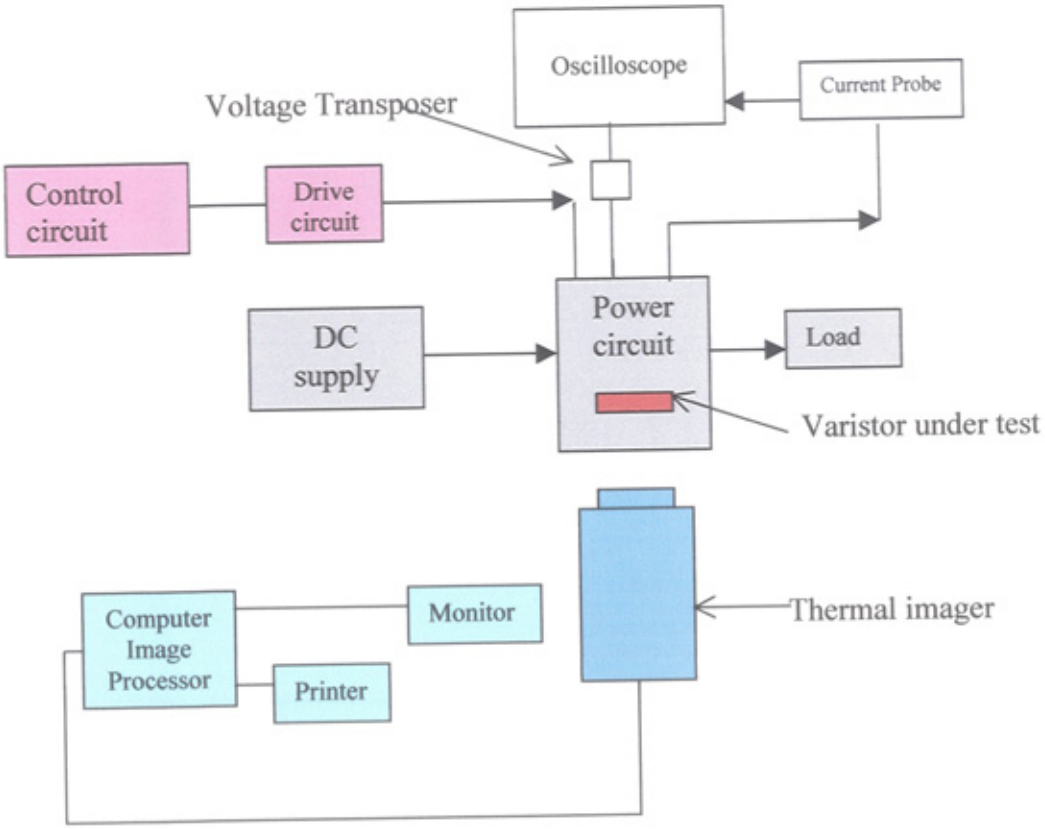


Figure 4.10 A schematic arrangement of the experimental system

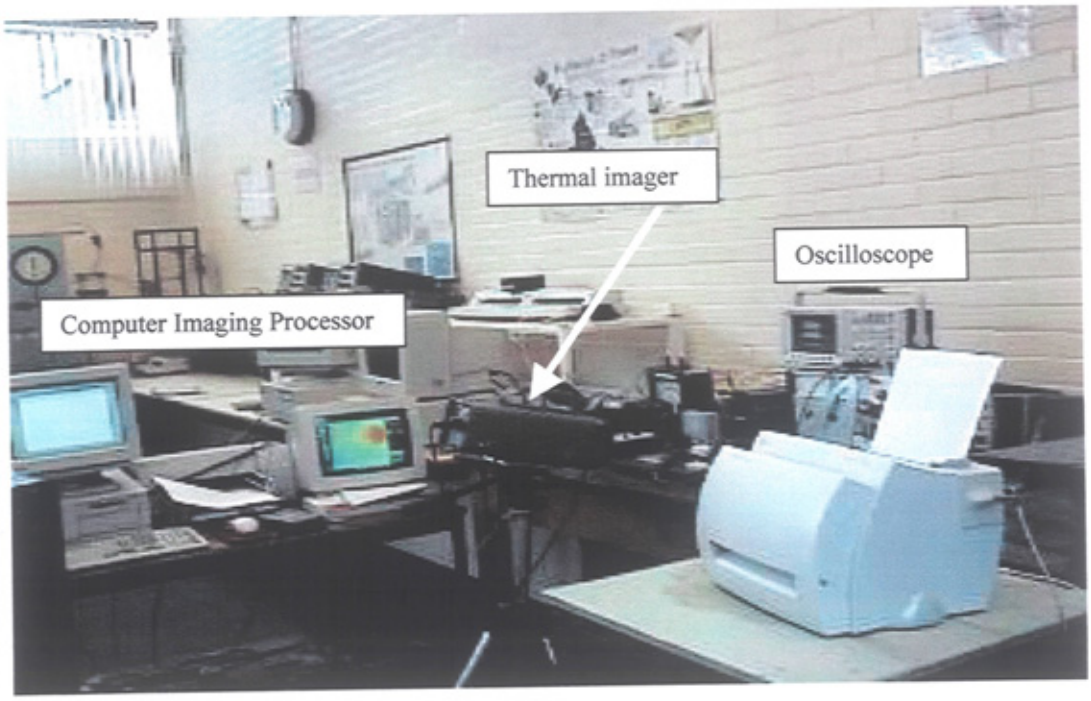


Figure 4.11 The experimental set up

Figure (4.12) shows the power circuit which, produces the current pulses to be injected in the varistor under test. The circuit consists of a d.c. supply (V1 = 250 V), an IGBT, a freewheeling diode (D1, to protect the IGBT from reverse voltage), a snubber circuit (R1, C1 and D2 to protect IGBT from high dv/dt), the test varistor (V), an RL load bank and a control circuit generate continuous repetitive pulses. Figure (4.13) shows the power circuit components assembled on one board in order to minimise the stray inductance.

When no triggering pulses are applied, the IGBT is off and the supply voltage (much lower than the varistor clamping voltage) appear across the varistor terminals. When the IGBT is turned on, the current starts to flow through the IGBT and energy is stored in the circuit inductance. When the IGBT is turned off, the inductance tries to maintain the flow of current producing high voltages across the IGBT and varistor. The current through an inductor cannot change abruptly, so it flows through the varistor initially with the value of the operating load current, then decaying exponentially toward zero, as shown in the APPENDIX A. The IGBT is turned on for a period of 540 μs and then is turned off for a period of 540 μs the process continues for a controllable pre-set duration.

Test results

Thermal images obtained at regular time intervals present a dynamic record of the thermal condition of the varistor. Figure (4.14) shows a group of thermal images for the 36 mm varistor (sample 1a) recorded at an interval of 80 ms for a total recording time of 480 ms. Recording started before IGBT operation which lasted for about 200 ms. The first image in Figure (4.14) shows the varistor at room temperature. During the first 240 ms. (images 2, 3 and 4), the varistor temperature increased rapidly to more than 127 °C at the hottest spot. Images 5 and 6 describe the temperature distribution after the

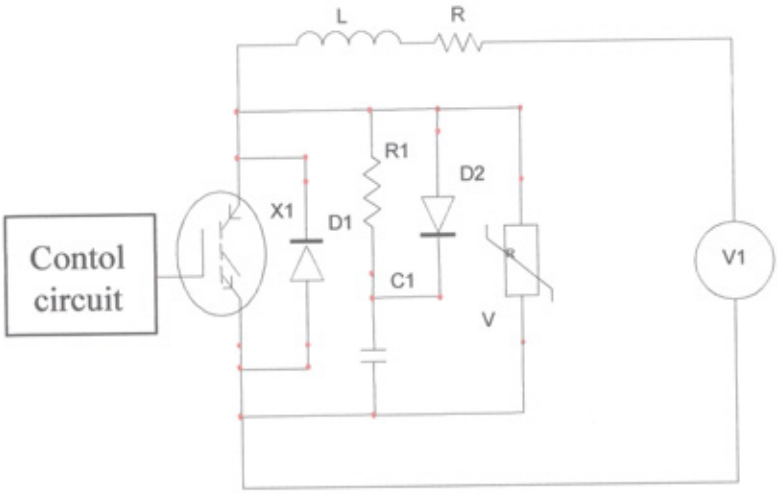


Figure 4.12 A schematic diagram of the test circuit

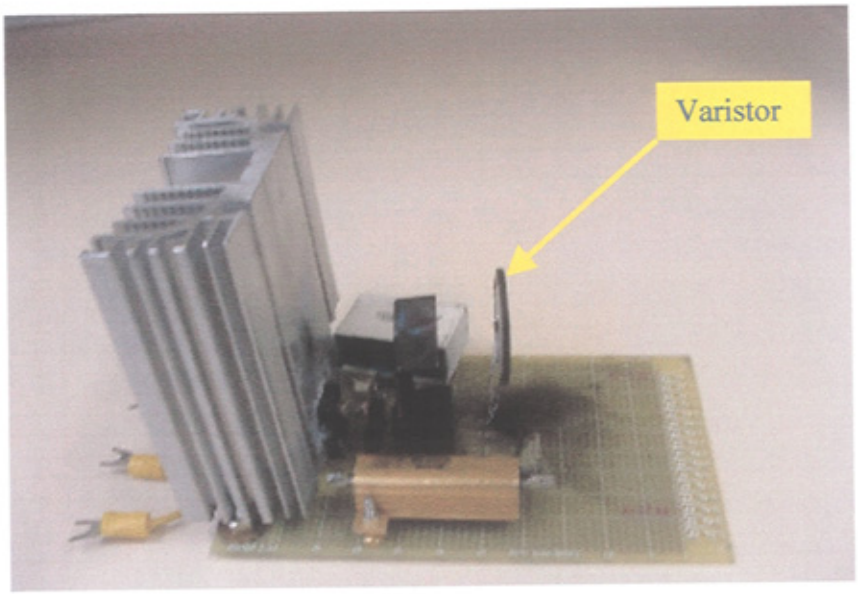
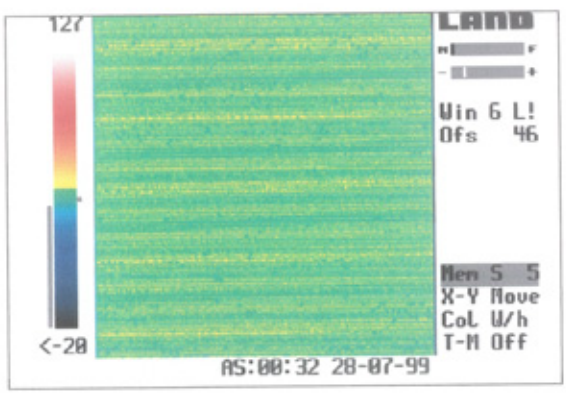


Figure 4.13 The power circuit

switching operation had stopped. The spread of heat from an initial small area can be seen. The images in Figure (4.14) show heat localisation with the hottest spot being to the right edge of the disc. The temperature there was higher than 127 °C (the temperature has exceeded the analysis window rating). In contrast, the coldest part of the varistor surface was in the region of 30 °C. Figure (4.15) shows the temperature distribution history of 36 mm (sample 1b) varistor. It is clear that the hot spot being to the right edge, such a large difference due to current localisation results in poor utilisation of the varistor volume. Similar tests were carried out on a 53 mm (sample 3) varistor. Figure (4.16) gives a group of thermal images of the varistor recorded at an interval of 80 ms. over a period of 480 ms.



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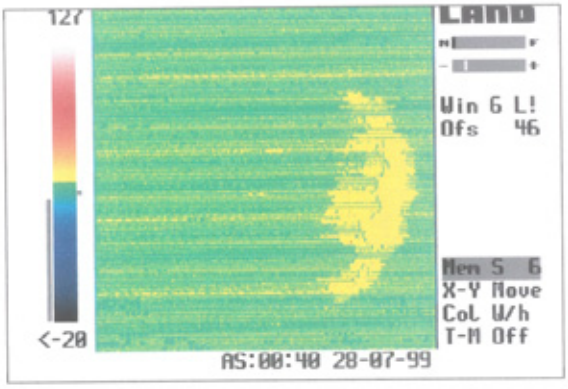

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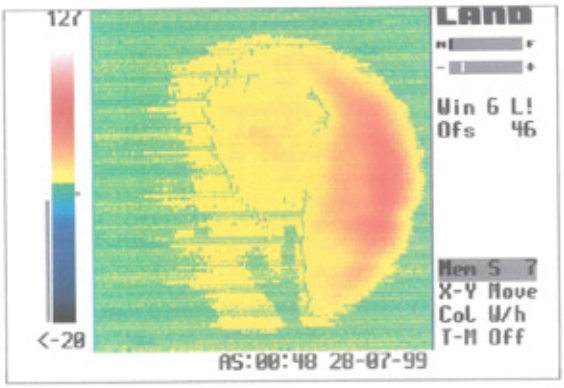

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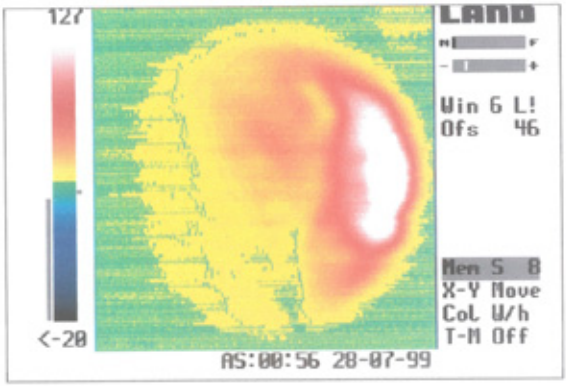

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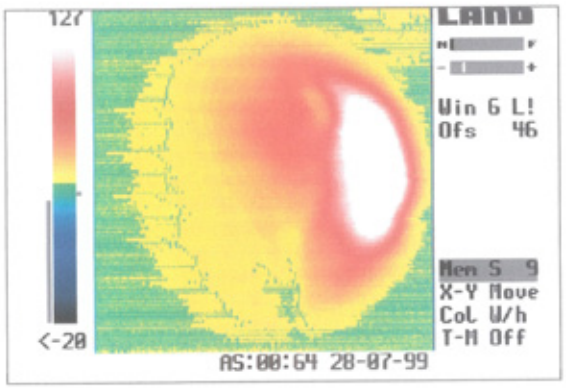

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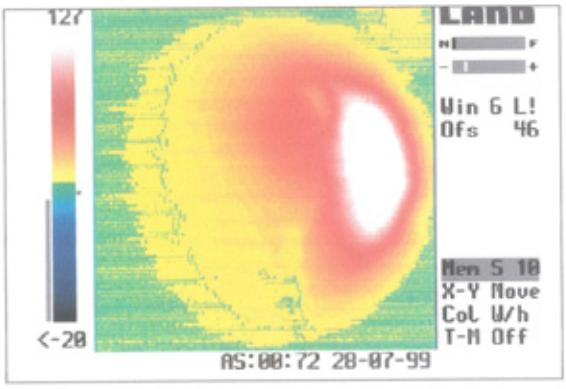

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Figure 4.14 Thermal images showing temperature distribution-time history in the 36 mm Varistor (sample 1a), (Continuous repetitive pulses for a period of 200 m sec)

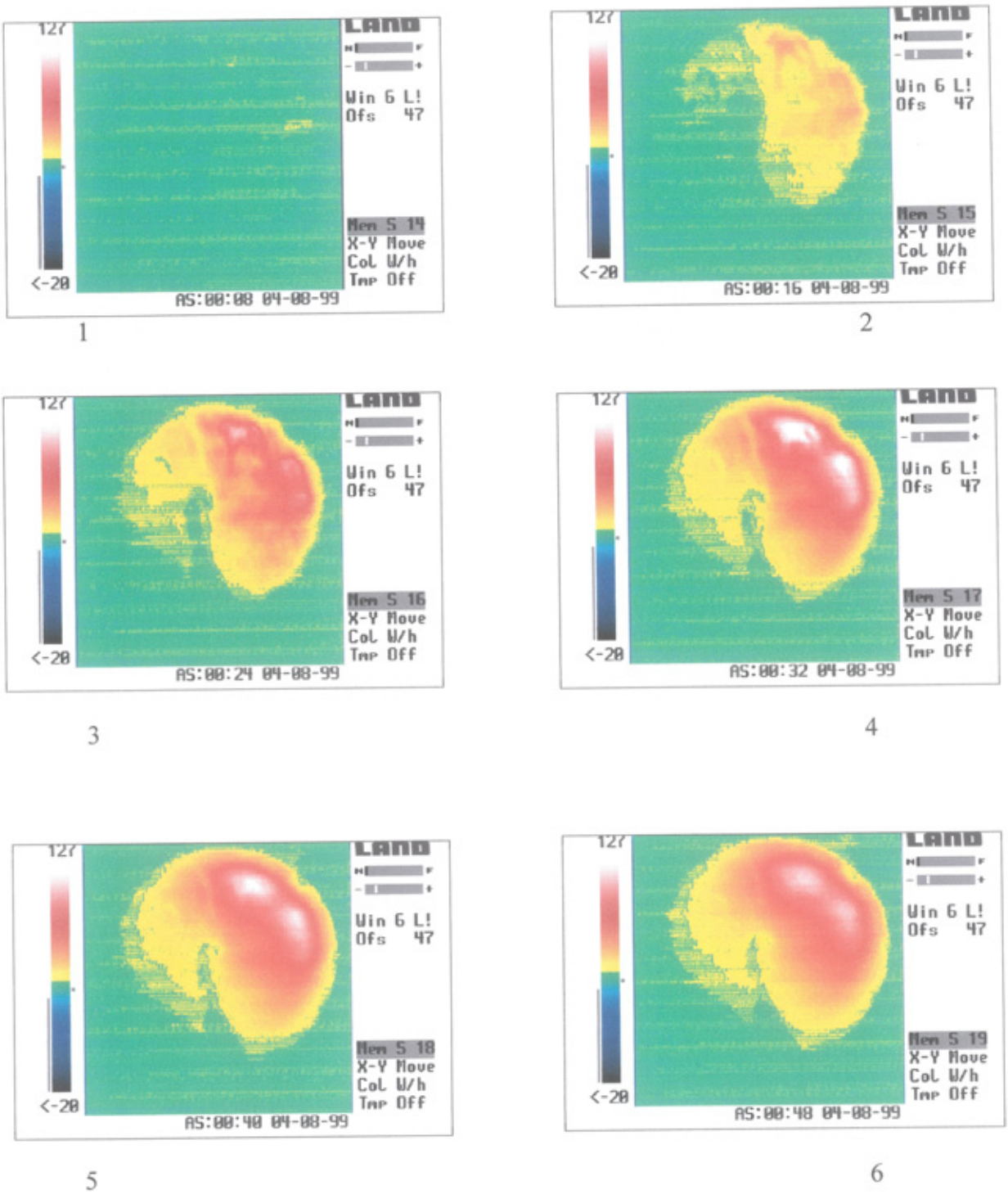
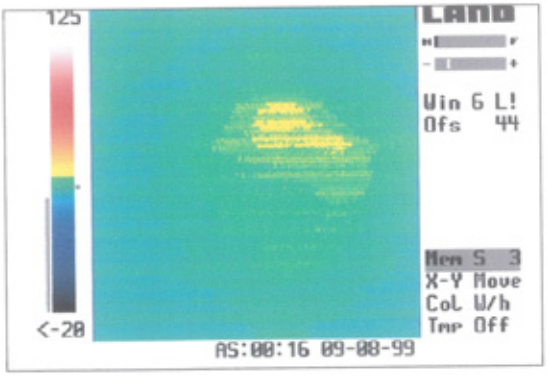


Figure 4.15 Thermal images showing temperature distribution-time history in the 36 mm Varistor (sample 1b), (Continuous repetitive pulses for a period of 200 m sec)



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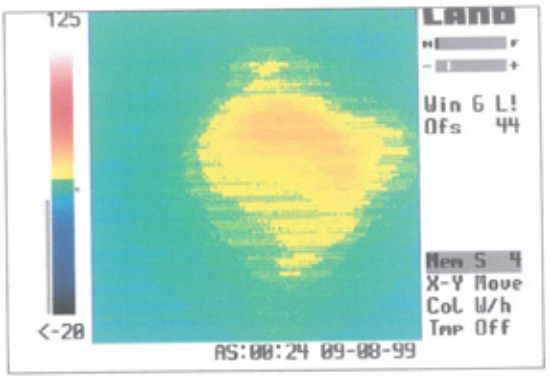

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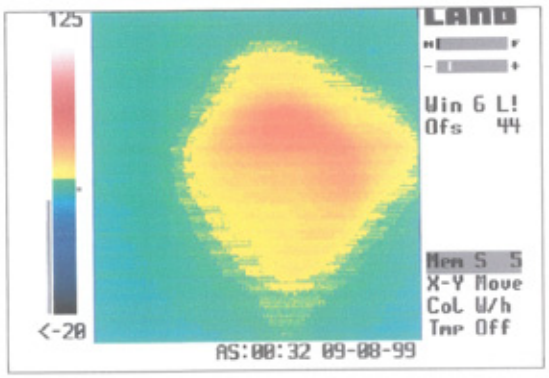

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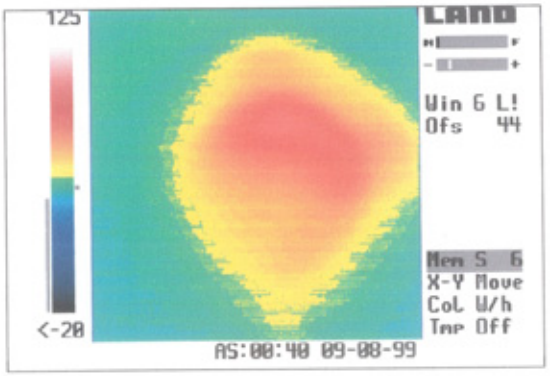

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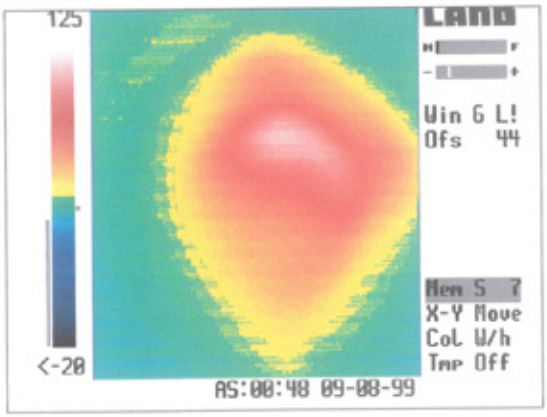

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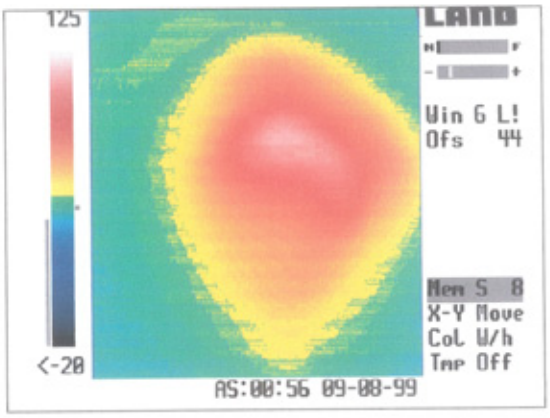


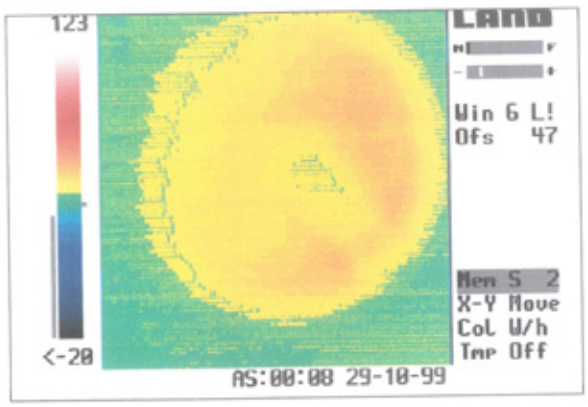
6

Figure 4.16 Thermal images showing temperature distribution-time history in the 53 mm Varistor (sample 3), (continuous repetitive pulses a for period of 400 m sec)

Continuous repetitive pulses were applied to the varistor for 400 ms. It is clear from the images shown that heat distribution is more uniform than the 36 mm (sample 1) varistor. A relatively mild current concentration spot was identified near the centre of the disc. Heat was evenly dissipated in all directions.

Similar tests were carried out on the 40 mm (sample 2) varistor. Figure (4.17) gives a group of thermal images of the 40 mm (sample 2) varistor. Continuous repetitive pulses are applied to the varistor for a period of 180 milliseconds.

It is clear that this 40 mm varistors is more uniform than the other types tested (36 mm and 53 mm) which confirm with the secondary electron images. This uniformity due to the well distribution of all phases, even with high porosity content as shown in Figure (4.5).



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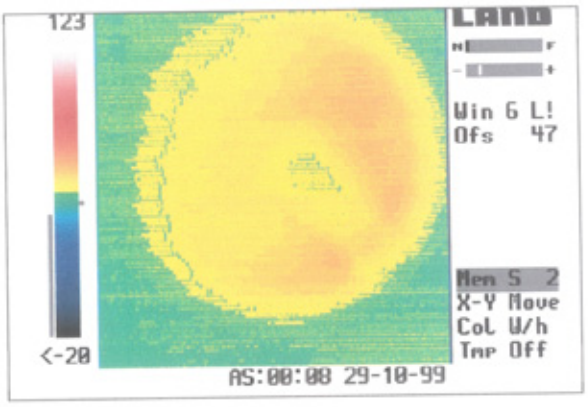

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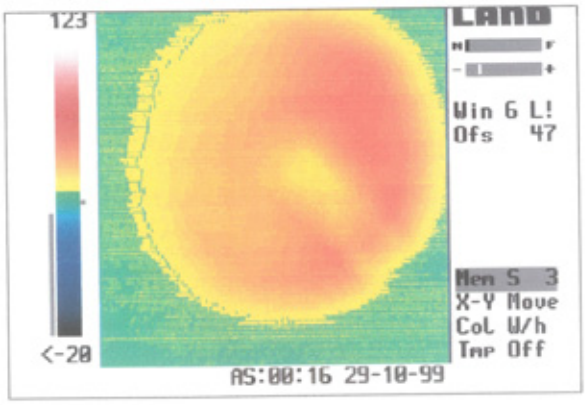

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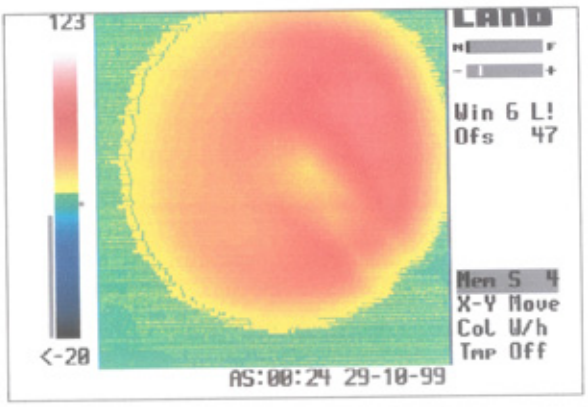

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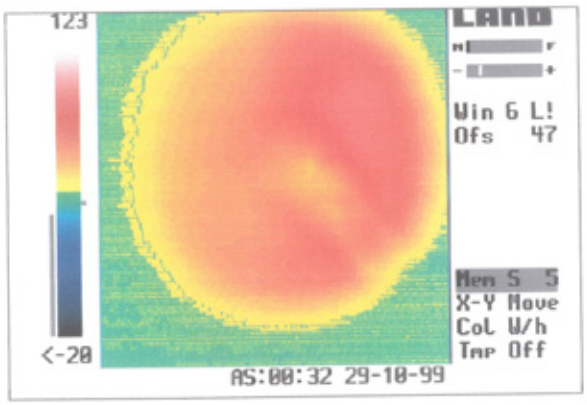

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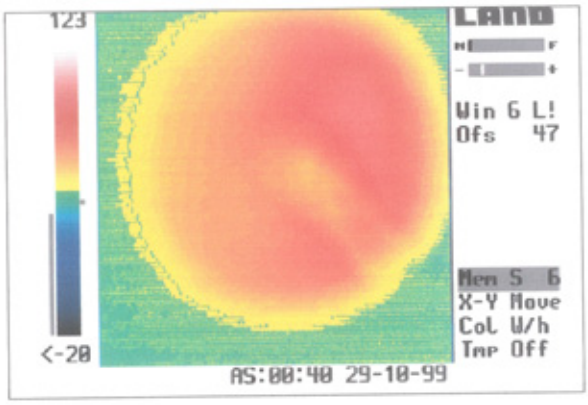

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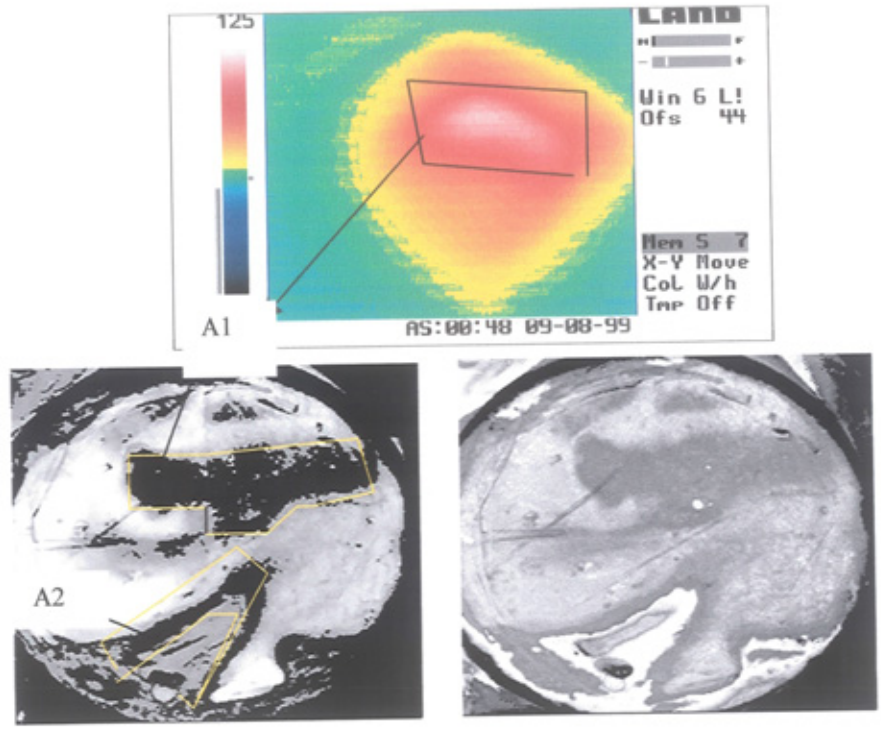
Figure 4.17 Thermal images showing temperature distribution-time history in the 40 mm Varistor (sample 2), (continuous repetitive pulses for a period of 180 m sec)

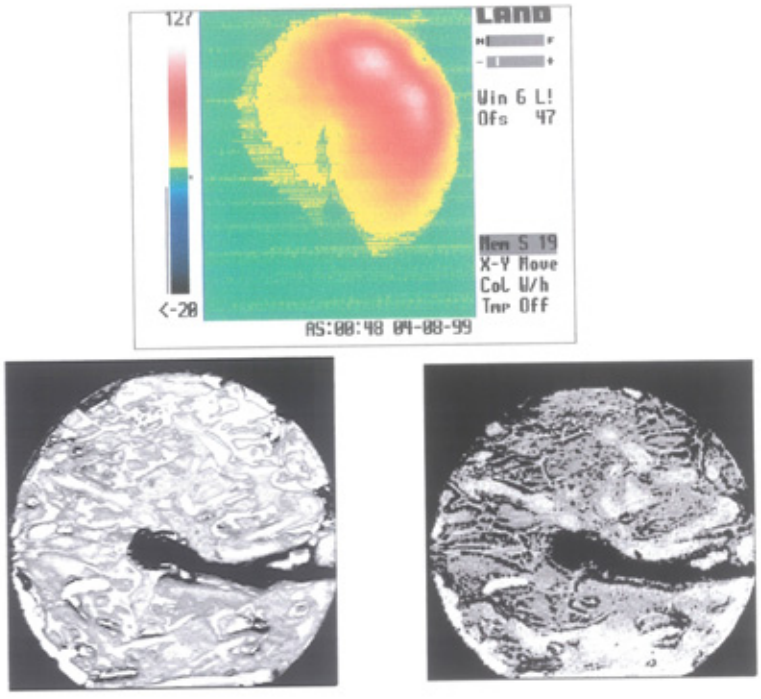
4.7 Non-destructive Tests Using Scanning Acoustic Microscope (SAM)

Ultrasonic is a commonly used mean of non-destructive testing. Pulses of compressional or shear pressure waves at frequencies of 1-100 MHz are generated by a piezoelectric transducer. The pulses pass through the specimen and reflections are picked up by the same transducer [72]. Each pulse is modified by the path taken and energy is reflected by material discontinuities. The Ultrasonic transducer cannot generally operate in air. Water is therefore used as a transparent medium between the transducer and the specimen to allow ultrasonic energy to transmit into and out of the specimen. Varistors to be tested are placed in trays in an immersion tank and the scanner is positioned to scan under computer control. Figures 4.18 and 4.19 show the images of the 53 mm (sample 3) varistor and 36 mm (sample 1) varistor, respectively scanned at different depths. The results obtained for each sample were compared with the corresponding thermal images of the same sample. For the sample 53 mm (sample 3) it is noticed that there is a match between area A1 taken by both techniques. For area A2 of sample 53 mm (sample 3) and images for sample 36 mm (sample 1) no conclusive match could be found. It can be concluded that the ultrasonic scanning microscope does not provide useful information for varistor microstructure uniformity.



L1 L2

Figure 4.18 Comparison between thermal images and SAM (varistor 53 mm)



L1 L2

Figure 4.19 Comparison between thermal images and SAM (varistor 36 mm)

4.8 Evaluating The Energy Handling Capability of The Varistor

Energy handling capability can be defined as the amount of energy that the varistor can absorb before it fails. Thermodynamically, the energy per unit volume that an ideal varistor is capable of absorbing is determined by the temperature rise due to the energy absorption, which is a function of its density and specific heat [73, 74].

$$J_{\max} = \rho \cdot C_p \cdot (T_2 - T_1) \ \text{J/cm}^3 \qquad (4.1)$$

where ρ = density, g/cm^3

C_p = specific heat, J / g °C

$T_2 - T_1$ = temperatue rise, °C

This theoretical relationship assumes that all of the heat generated is absorbed by the varistor and that none is dissipated to the environment. For the MOV, $C_p \approx 0.89$ J/g °C at 25 °C and $C_p \approx 1.0$ J/g °C at 130 °C. The theoretical density is 5.60 g/cm^3. Hence the volumetric specific heats are 4.98 and 5.60 J/cm^3 °C, at the above two temperatures, respectively. Thus, a 100 °C temperature rise corresponds to about 500 J/cm^3. The specified energy levels of practical MOV's fall between 200 and 250 J/cm^3.

According to the above, it is obvious that the theoretical energy handling capability of an ideal varistor is directly proportional to its volume. For MOV to operate without failure or degradation, it must quickly dissipate the absorbed energy and return to its pre-pulse design ambient temperature. The duration of operation, its frequency of occurrence, the geometry of the device, and the operating environment determine the rate of heat dissipation.

In order to define the maximum continuous energy that a varistor can absorb without any damage, several tests were performed on three more samples of the 53 mm (sample 3)

type varistor using thermal imaging system. For each sample, thermal images before, during and after the switching operation were recorded. Operation time was varied to change the energy absorbed by the varistor. In each case, the maximum surface temperature of the varistor was monitored. Figure (4.20) shows, for the three samples, the relationship between the maximum temperature (Tmax) and the switching operation time. Figure (4.21) shows the relationship between the energy absorption of the varistors (calculated as $\int v\, I\, dt$) and operation time.

The relationship of varistor temperature versus input energy is derived from Figures (4.20 and 4.21) and is shown in Figure (4.22). In all these tests, the maximum surface temperature of the varistors was raised to about 200°C without causing any damage. Comparing with the specification in Table 4.1 (page 80), it is shown that the varistor maximum temperature remains under 200 °C even when the total energy absorbed is about twice the "maximum energy absorption" (880 J). It is clear that the varistor can operate with continuous repetitive pulses safely as long as its thermal stability point is not reached. This is because the off periods of the pluses allow some heat to dissipate through the bulk of the varistor.

For certain tests, the switching time was increased gradually until the varistor fails (puncture mode) due to presence of microstructure non-uniform current localisation. Increasing the switching time leads to temperature rise along current localisation path. The local temperature increases leading to further and continued current localisation and in turn further heating. Further increase in the switching time, results in the varistor failure and its electrodes be shorted.

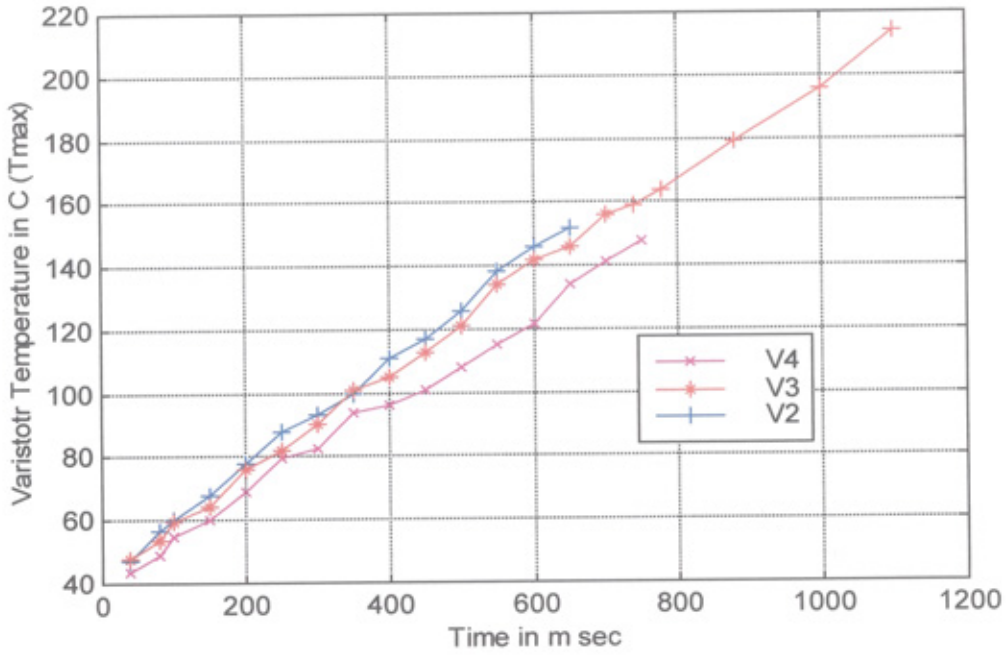


Figure 4.20 The relationship between the Varistor maximum temperature and switching period

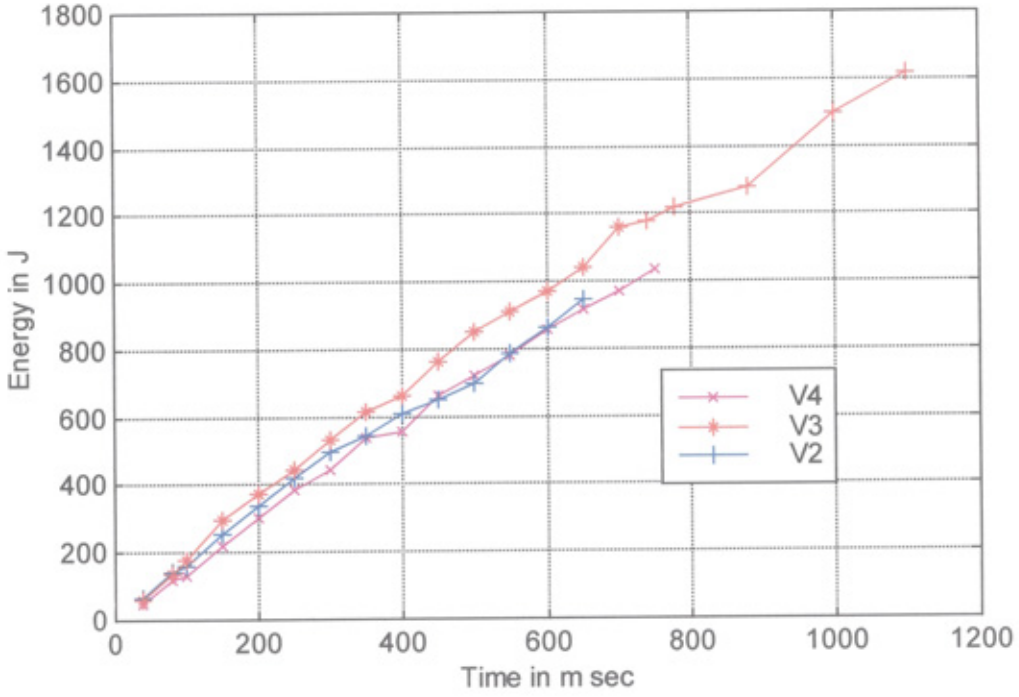


Figure 4.21 The relationship between the Varistor energy and switching period

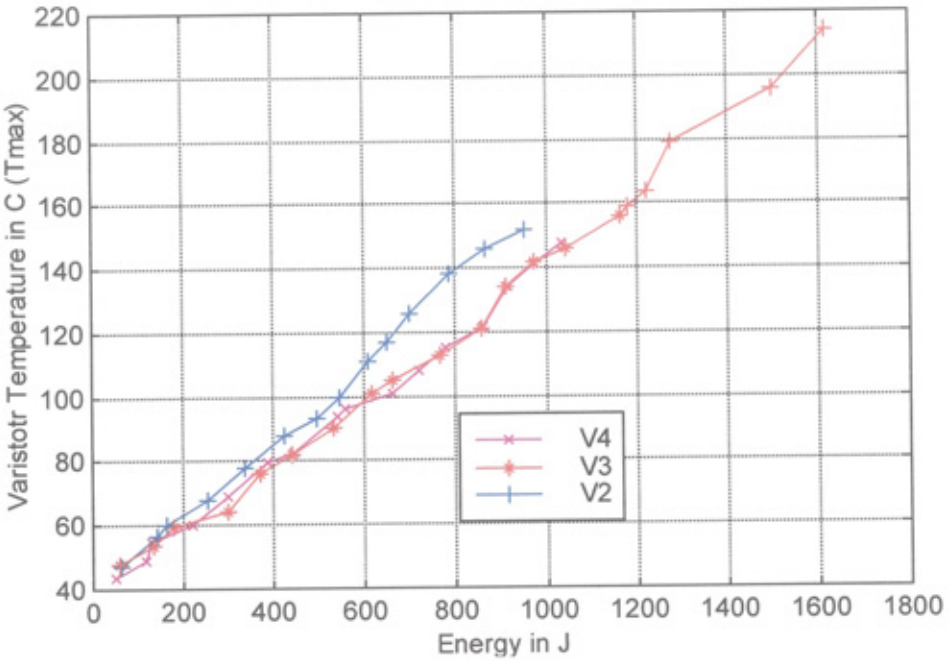


Figure 4.22 The relationship between the Varistor temperature and energy.

As show in Figure (4.23), three thermal regions can be identified. Firstly there is the thermal stability region in which the varistor maximum surface temperature is proportional to the input energy to the varistor. Secondly, there is the region "out of thermal stability", where a small increase in the input energy leads to large temperature rise. Finally, there is the thermal runaway region where the hot spot temperature increases until local varistor puncture occurs. For the FCLID, keeping the total energy absorbed by the varistor near the value given in the varistor specifications (per pulse) will result in a conservative safe operation.

The experimental results show that the varistors can be used for continuous repetitive pulses within their energy rating per pulse as specified in the manufacturers data sheet. This capability is limited by one of the failures mechanism (puncture) of the varistors and is not sufficient for the FCLID operation. One way to increase the energy handling capability is to connect varistors in parallel.

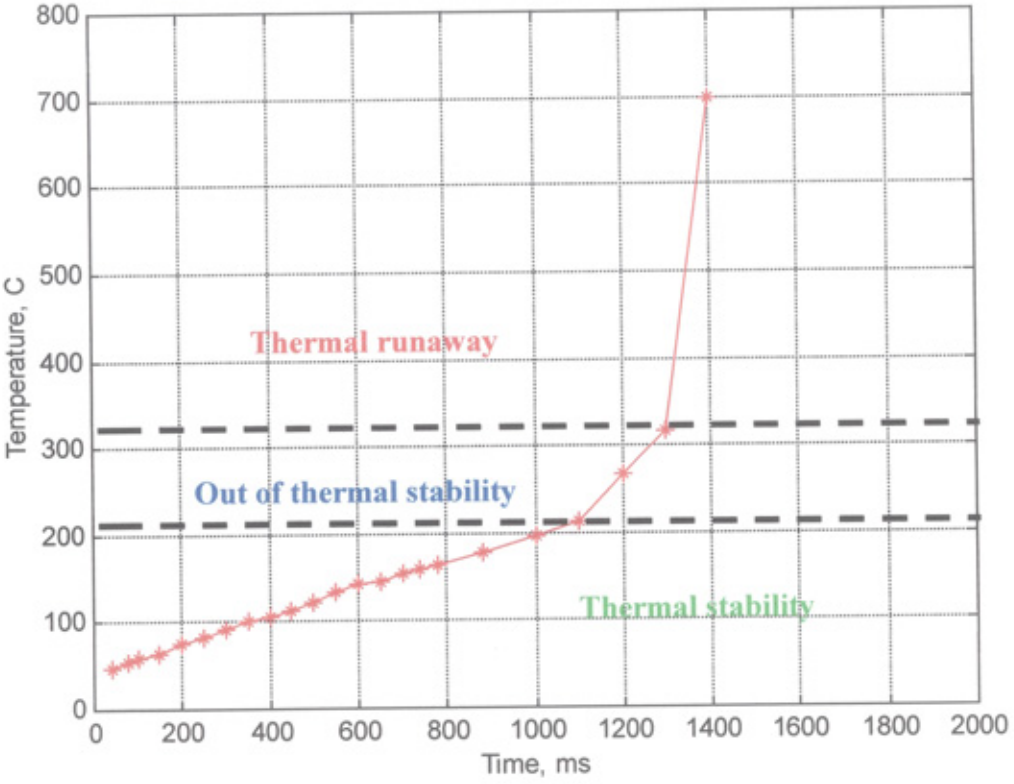


Figure 4.23 Thermal runaway

4.9 Improving Current Sharing Between Parallel Varistors

Commercially available varistors are intended for operation during a very short period of time, e.g. a few ms. The FCLID operation is to be maintained for a period of few seconds. Thus, power dissipation in the varistors can be very excessive. Consequently, several varistors connected in parallel are necessary to achieve the required energy rating. Due to their non-linear characteristics, the amount of current flow in each parallel varistor is very sensitive to variations in the applied voltage. Therefore, a small variation in the characteristics of parallel varistors of the same type (within the manufacturer's normal tolerance) may lead to significant difference in their currents [75].

A method, suitable for the FCLID application, is used to improve the current sharing between parallel varistors without affecting their dynamic characteristics.

In this method, each varistor is connected in series with a small power resistor, which may have the same value R, as shown in Figure (4.24).

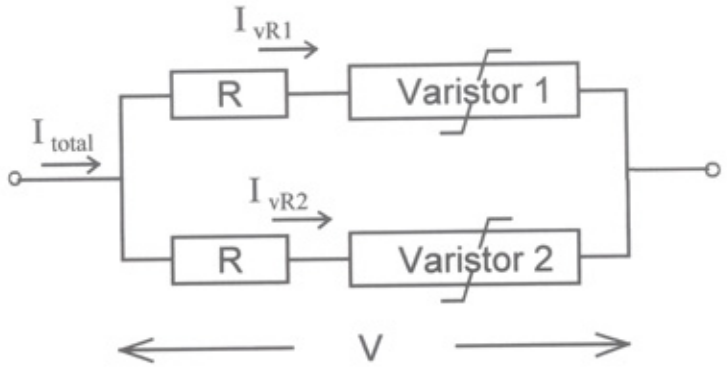


Figure 4.24 Parallel operation

The current sharing, without the resistance R, can vary depending on the varistor characteristics illustrated in Figure (4.25). If the clamping voltage V_a is applied the current in each varistor may be calculated as:

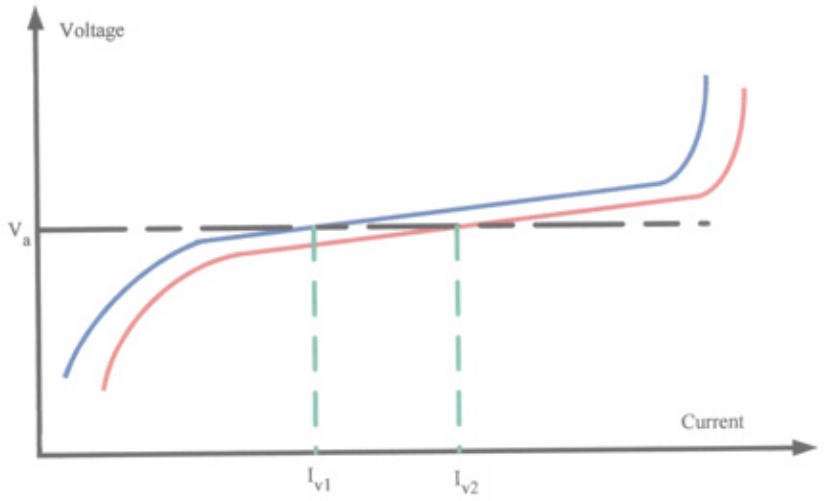


Figure 4.25 Varistor characteristics (can be assumed linear in the conduction region)

$$I_{v1} = \frac{V_a}{\alpha \cdot K_1} \tag{4.2}$$

$$I_{v2} = \frac{V_a}{\alpha \cdot K_2} \tag{4.3}$$

where α is the non-linear exponent of the varistor

K_1 and K_2 are the dynamic resistances of the two varistors during the conduction period, i.e. dV/dI. K_1 and K_2 are normally small [62].

The total current is equal to:

$$I_{total} = I_{v1} + I_{v2} = \frac{V_a}{\alpha \cdot K_1} + \frac{V_a}{\alpha \cdot K_2} \tag{4.4}$$

$$I_{total} = V_a\left(\frac{\alpha \cdot K_2 + \alpha \cdot K_1}{\alpha \cdot \alpha \cdot K_1 \cdot K_2}\right) = V_a\left(\frac{K_2 + K_1}{\alpha \cdot K_1 \cdot K_2}\right) \tag{4.5}$$

Similarly, the total current through the varistors when the series resistances are connected may be found as:

$$I'_{total} = I_{vR1} + I_{vR2} = \frac{V_b}{R + \alpha K_1} + \frac{V_b}{R + \alpha K_2} \tag{4.6}$$

where V_b is the new voltage across the circuit.

$$I'_{total} = V_b\left(\frac{R + \alpha \cdot K_2 + R + \alpha \cdot K_2}{(R + \alpha \cdot K_1) \cdot (R + \alpha \cdot K_2)}\right) = \tag{4.7}$$

if $K_1 = K_2$

$$= V_b\left(\frac{2 \cdot (R + \alpha \cdot K)}{(R + \alpha \cdot K) \cdot (R + \alpha \cdot K)}\right) = V_b\left(\frac{2}{R + \alpha \cdot K}\right) \tag{4.8}$$

In the FCLID application, the total current in the parallel varistors is constant. In order for the total current in equation (4.8) to be the same as that given by equation (4.5), the operating voltage of the circuit V_b will have to be higher than V_a.

The percentage increase in the operating voltage relative to the clamping voltage is given as:

$$\frac{V_b - V_a}{V_a} \times 100\% = \frac{I_{total} \cdot \left(\frac{R + \alpha \cdot K}{2}\right) - \left(\frac{\alpha \cdot K}{2}\right)}{V_a} = \frac{I_{total} \cdot R}{2 \cdot V_a} \times 100\% \tag{4.9}$$

As the added resistance R is significantly higher than the dynamic resistance K of the varistor, it will dominate the current sharing. The difference in the current between the two varistors in both cases (without and with series resistance) can be found as:

$$I_{v1} - I_{v2} \approx V_a \cdot \left(\frac{K_2 - K_1}{\alpha \cdot K_1 \cdot K_2}\right) \tag{4.10}$$

$$I'_{v1} - I'_{v2} \approx V_b \cdot \left(\frac{\alpha \cdot (K_2 - K_1)}{R^2 + \alpha \cdot R \cdot K_1 + \alpha \cdot R \cdot K_2 + \alpha^2 \cdot K_1 \cdot K_2}\right) \tag{4.11}$$

It can be deduced from (4.11) that by adding the series resistance, the difference between the two varistor's currents is reduced. Also, the larger is the added series resistance, the more uniform will be the current sharing at the expense of higher operating voltage.

4.9.1 Simulation results

To validate the above principles, the circuit shown in Figure (4.24) was simulated using MATLAB/SIMULINK software package. The varistor is modelled by a combination of three exponential functions of the form:

$$I = K_i V^{\alpha_i}$$

Two varistors have been connected in parallel in the circuit shown in Figure (4.12), the IGBT is switched continuously on and off at 1.1 kHz with a duty ratio of 0.5. Each time the IGBT is turned off, the current is diverted to the varistors. When the stored energy is dissipated in the varistors, the circuit current decreases to zero for the rest of the switching cycle (as the supply voltage is lower than the varistor clamping voltage ≈ 650 V). Without implementing the series resistors, the current waveforms

through the varistors are not uniform, as shown in Figure (4.26). Figure (4.27) shows the improvement in the current sharing when a 1 Ω resistor is connected in series with each varistor.

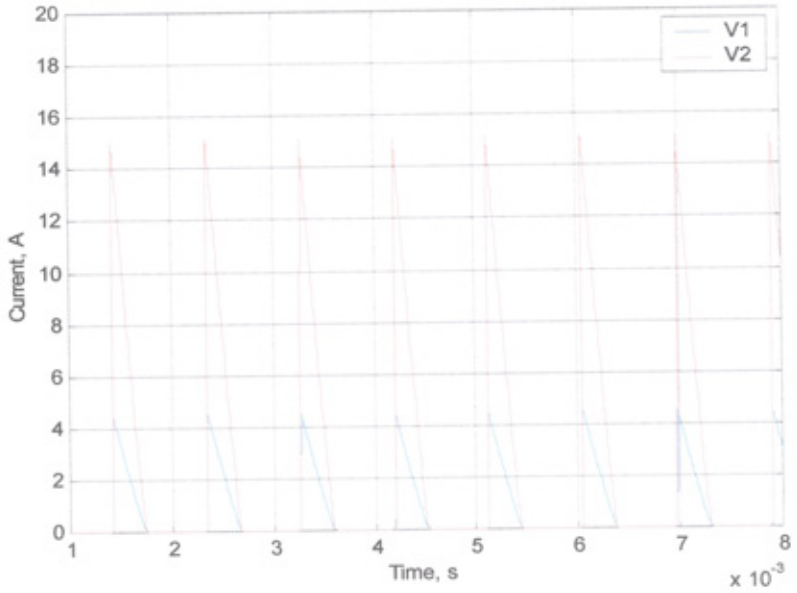


Figure 4.26 Current waveforms in varistors without series resistors

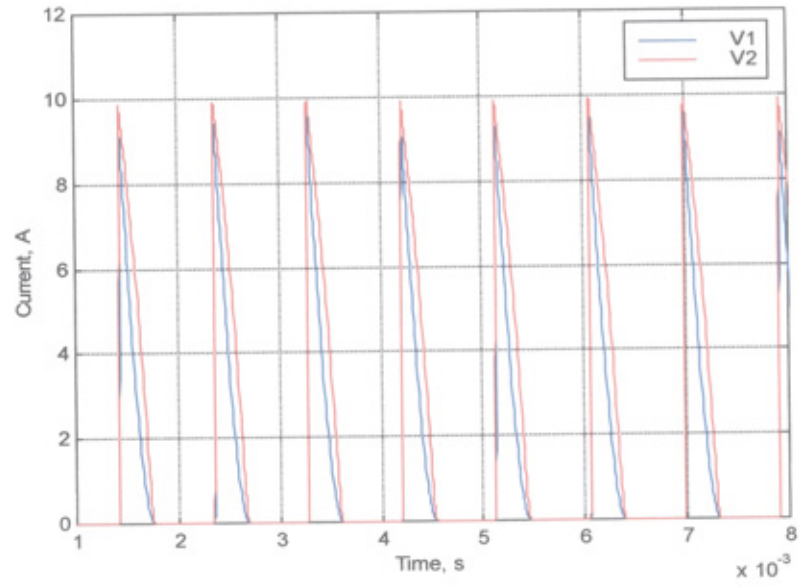


Figure 4.27 Current waveforms in varistors with series resistors

4.9.2 Experimental results

Two varistors have been connected in parallel in the circuit shown in Figure (4.13), to verify the simulation results. With no series resistance, Figure (4.28) shows the voltage waveform as measured across the two varistors and the current waveforms in each one. The current waveforms show that the sharing between the two varistors is indeed very poor. The unequal current sharing is confirmed using an infrared camera to image the temperature distribution on the varistors surfaces during operation. Figure (4.29) shows the image after operating for 400 ms. It is clear that the varistor which carries more current is heated up to a higher temperature. When a 1 Ω resistor is connected with each of the varistors, the measured voltage and current waveforms are modified, as shown in Figure (4.30). Compared with Figure (4.28), the amplitude of the voltage is slightly increased from about 650 V to 657 V. Also, while the total current in both cases is the same (~20 A, peak), the current sharing in Figure (4.30) is almost equal. Figure (4.31) shows the thermal image of the two varistors after operating for 400 ms. In this case, the two varistors are heated up to a similar level and the highest temperature is lower than that shown in Figure (4.30) although the operating time load level are the same in both cases. As the current sharing can be improved, it is possible to connect a number of varistors in parallel to achieve the required rating. Eight varistor have been connected in parallel to achieve the energy required for the FCLID to operate for period up to 1 s as explained in Chapter 5.

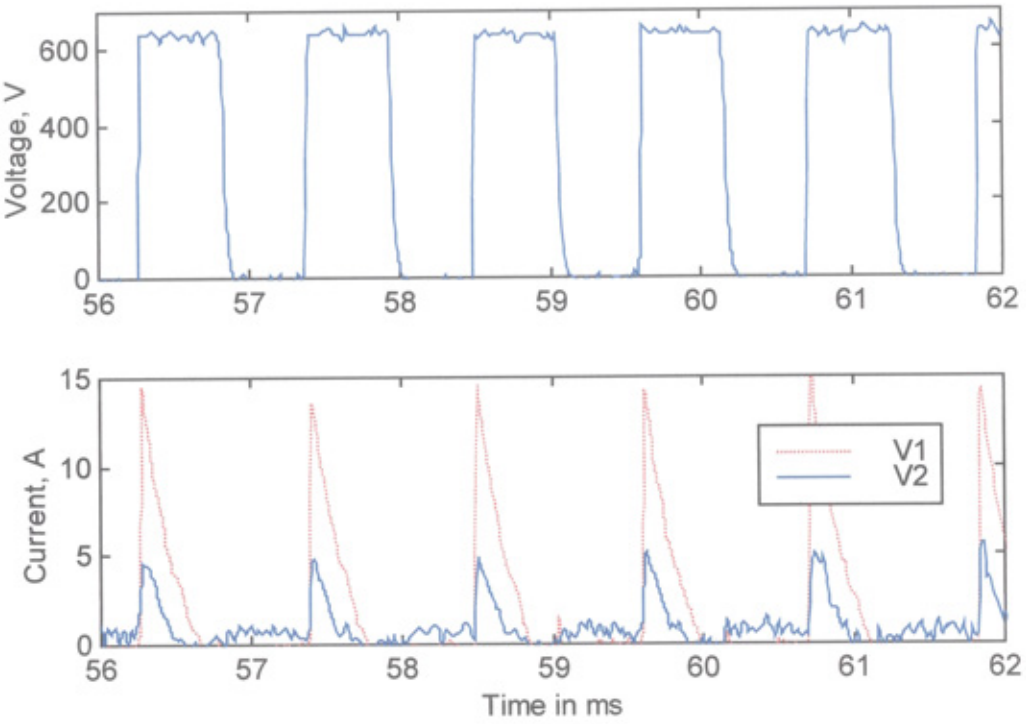


Figure 4.28 Voltage and current waveforms without series resistors

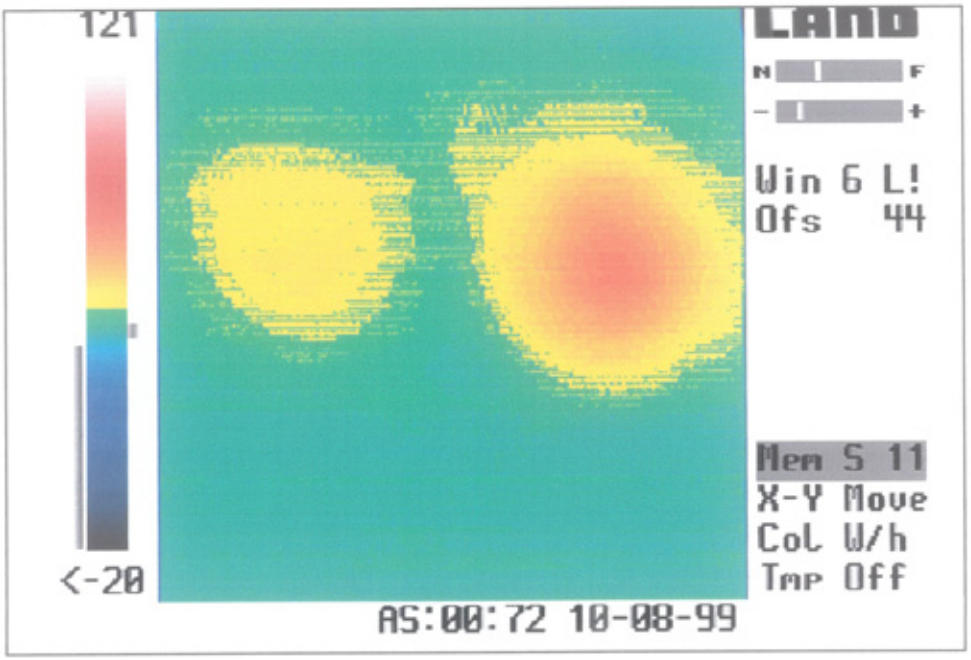


Figure 4.29 Thermal Image of the parallel varistor without series resistors

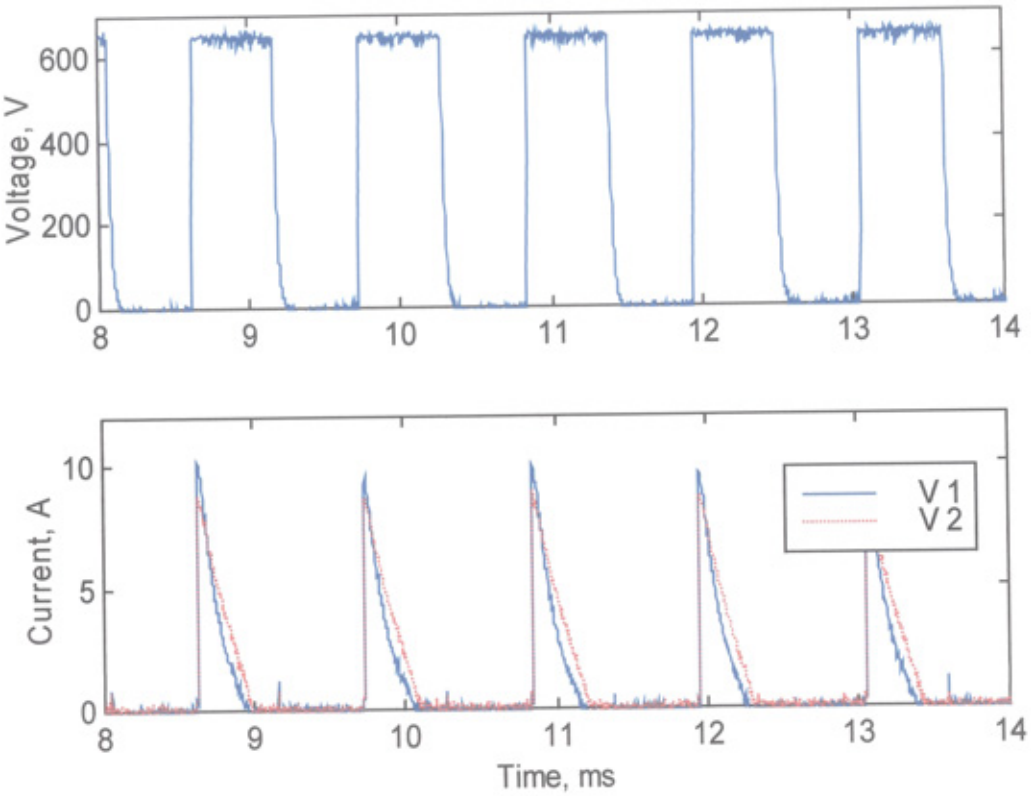


Figure 4.30 Voltage and current waveforms with series resistors

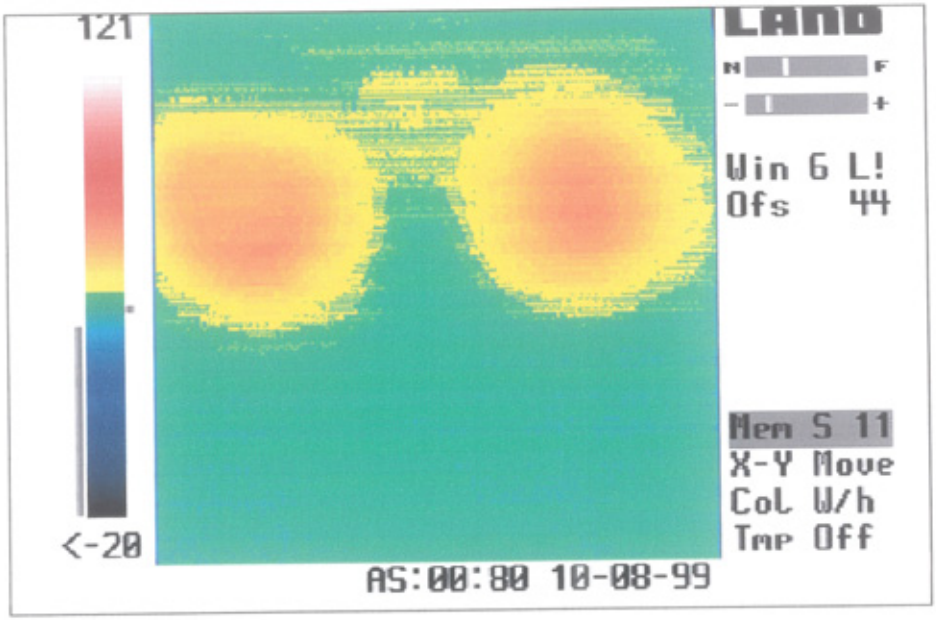


Figure 4.31 Thermal image of the parallel varistor with series resistors

4.10 Measuring Varistor Temperature

In practice the operating condition of the FCLID is not fixed and the energy input to the varistor may result in exceeding the thermal stability region of the varistor, so it is necessary to measure the varistor temperature during the FCLID operation. From the literature survey on the temperature measurement there are three commercially available devices that have been used for measuring the temperature of a component: a thermocouple, an infrared camera and a distributed temperature sensor. The thermocouple has a low response and can't be used for measuring the temperature distribution over the varistor surface. Both the infrared and distributed temperature sensors are very expensive. For this reason a new method is proposed.

The principle of operation of this method is obtained from the relationship between the input energy to the varistor and maximum varistor temperature shown in Figure (4.23). It is clear that this relationship is linear up to the thermal stability limit. Figure (4.32) shows the basic circuit of the proposed method for measuring the varistor temperature. So the input energy to the varistor is measured and compared with a reference value (energy rated per pulse for the varistor). A signal to trip the FCLID operation is generated if the measured value exceed the reference value. In such case the temperature of the varistor will not exceed the thermal stability region (190 °C -220 °C), based on the manufacture safety factor. The FCLID operating time can be predicted by measuring the input energy to the varistors for one cycle in the same way as described in Chapter 3. The FCLID operating time can be found as:

$$FCLID_{time} = \frac{E_{total}}{E_{1\ cycle}} \text{x } .02 \text{ s} \qquad (4.12)$$

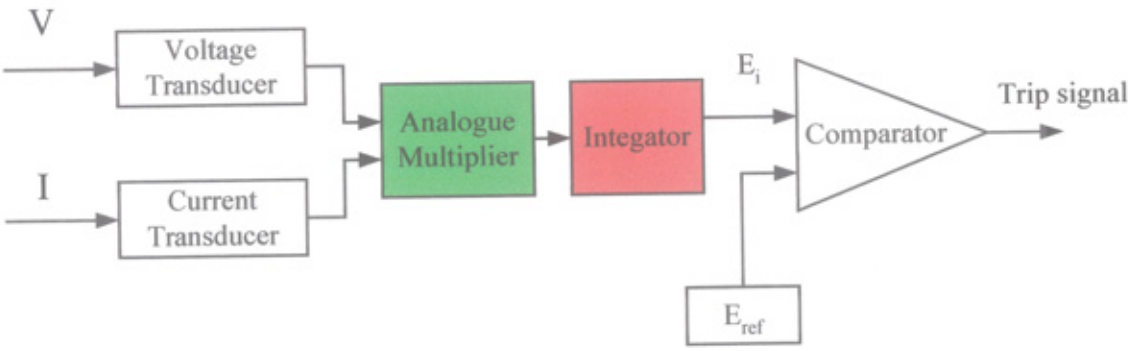


Figure 4.32 Basic circuit for varistor temperature measurements

4.11 Conclusions

Three methods have been used to study the uniformity of varistors; two destructive methods using Scanning Electron Microscope and infrared thermal imaging system and one non-destructive method using Acoustic scanning microscope.

The energy handling capability of ZnO varistors has been examined. The results obtained show that:

- The infrared imaging system is a useful means for measuring the energy handling capability, temperature distribution and uniformity of the microstructure of the varistor.
- The acoustic scanning microscopy does not provide useful information for measuring the uniformity of the varistor microstructure. However, it can be used to find structural defects.
- Achieving the maximum energy handling capability of a varistor strongly depends on the varistor microstructure uniformity; the more uniform, the better is the energy handling capability.

- When subjected to continuous repetitive pulses the varistor can handle a total energy higher than the rating usually specified in data sheets for a single pulse.
- There are three characteristics regions prior to varistor puncture: the thermal stability region, the out of thermal stability region and the thermal runaway region.
- The energy rating of commercially available varistors is not enough to operate the FCLID for the specified rating. In order to achieve the energy rating required, parallel operation of varistors is necessary.
- A new method is proposed to improve the current sharing when operating Metal oxide varistors in parallel. It is shown that improved current sharing is achieved by connecting a small resistor in series with each varistor. The effects of the additional series resistors on the overall V-I characteristic and the clamping voltage have been analysed. The proposed method has been experimentally verified and is relatively easy to implement.
- A new method for measuring the varistor temperature has been suggested. Using this method will protect the varistors of the FCLID from overheating when system operating conditions change.

CHAPTER FIVE

DEVELOPMENT OF THE FCLID PROTOTYPE

5.1 Design f The Gate driver and Snubber Circuits

The design of the snubber components depends on the operating conditions and on the semiconductor component itself. As a consequence, the snubber has an influence on the turn off loss in the semiconductor switch. It is the purpose of the present section to summarise the turn-off process of the IGBT under the FCLID operation and to present a design procedure for an optimised snubber. For a given turn-off voltage and a given component voltage limit, the optimisation lead to minimum snubber capacitance, which reduces cost, space requirements and power loss.

Figure (5.1) shows a complete turn-off snubber circuit used for the FCLID. It comprises a capacitor-resistor combination across the FCLID terminals in parallel with the varistor. During the FCLID, the IGBT is turned off at current (Imax) and the current is diverted into snubber capacitor via resistor, while the collector current decreases. The transistor collector voltage is clamped to the varistor maximum clamping voltage, which is initially zero. The larger the capacitor the slower the collector voltage rises for a given varistor maximum clamping voltage and maximum interrupted current.

$$\frac{I_{\max}}{C_s} = \frac{dv}{dt} \qquad (5.1)$$

where: *Imax* is the maximum interrupted current by the IGBT.

C_s is the snubber capacitor.

dv = Vc – Vi

Vc is the maximum clamping voltage of the varistor.

Vi is the initial voltage across the capacitor

dt is the falling time of the IGBT

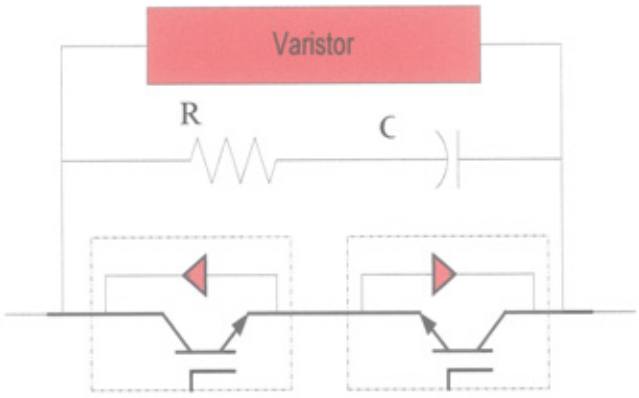


Figure 5.1 Complete snubber circuit for the FCLID

The energy storing capability in the capacitor depends upon the current interruption and varistor clamping voltage is used to limit the magnitude and rate of rise of voltage across the switch, providing the capacitor peak voltage limit is not exceeded. This energy is

$$\frac{1}{2} \cdot C_s \cdot V_c^2 \tag{5.2}$$

subsequently dissipated as heat in snubber resistor at transistor turn on, when an RC discharge occurs. If the snubber RC time constant is significantly shorter than the voltage fall time at turn on the capacitor energy dissipated in the resistor is less than $\frac{1}{2} \cdot C_s \cdot V_c^2$. The capacitor energy is removed at turn on and is dissipated mainly in the snubber circuit resistor. The power rating of this resistor is dependent on the maximum switching frequency and is given by:

$$P = \frac{1}{2} \cdot C_s \cdot V_c^2 \cdot f_s \,(\mathrm{W}) \tag{5.3}$$

where: P is the power loss in the snubber resistor and f_s switching frequency of the FCLID. There are two factors that specify the snubber circuit resistance value.

- The initial resistor current at the capacitor discharge is given by

$$\frac{V_{\text{supply}}}{R_s}$$

where V_{supply} is the supply voltage and R_s is the snubber resistor.

This component is added to the load current at turn on, hence adding to the turn on stress. Thus, the maximum collector current rating must not be exceeded.

- The snubber circuit RC time constant must ensure that after turn on the capacitor discharges before the next turn off is required. If Ton is the minimum transistor on time, then $t_{on(\min)} = 5 \cdot R_s \cdot C_s$ is sufficient to ensure correct snubber circuit initial conditions. The parameters of the designed snubber circuit are listed in Table (5.1).

The most expensive and vulnerable devices in FCLID applications are the semiconductor keys i.e. IGBTs. Especially limited voltage and current values as well as power losses are not to be exceeded. Therefore it is important for the IGBTs gate driver to fulfil various requirements. The most important are:

- Galvanic separation between control and power circuits.
- IGBT protection against short-circuit and destruction of the transistor.
- Low and limited supply current consumption.
- Protection against supply voltage deviation
- Generation of error signals.

The hybrid signal IGBT SEMIKRON SKHI 10 driver unit was used for this study. Figures 5.2 & 5.3 show the functional block diagram and the experimental circuit of the SKHI 10.

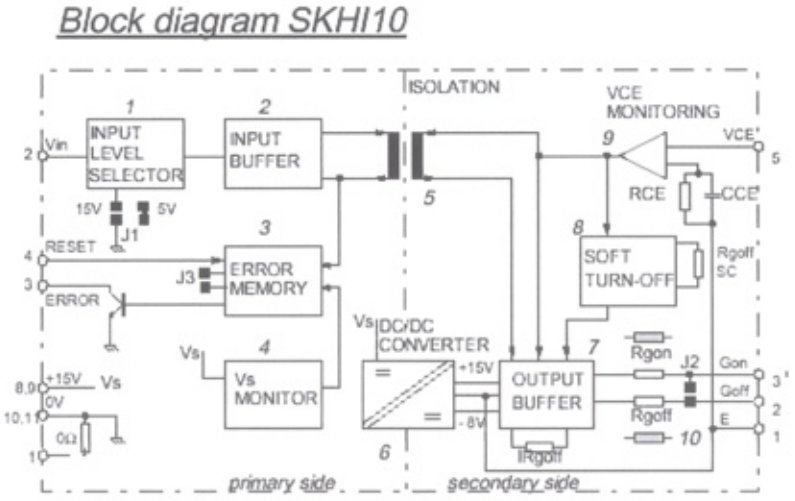


Figure 5.2 Block diagram of the IGBT gate driver

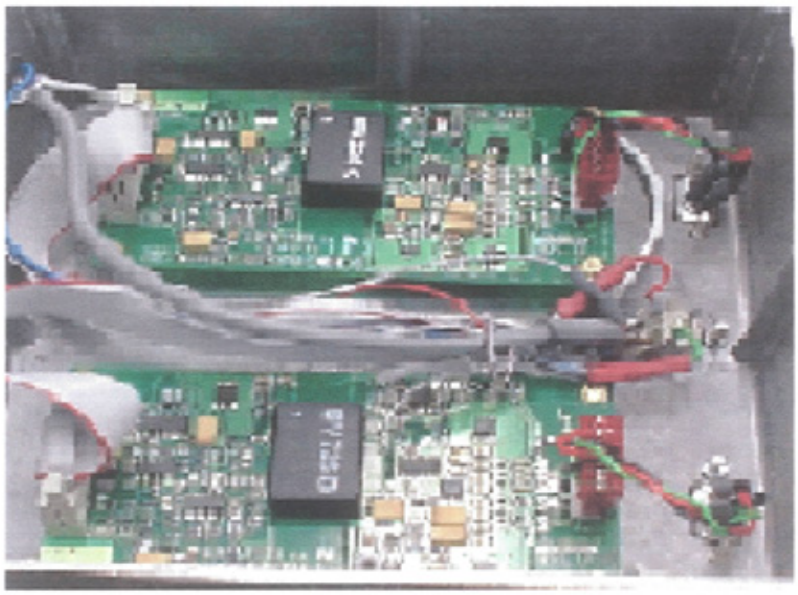


Figure 5.3 IGBT gate drivers

5.2 Design of The FCLID Controller

The function of the FCLID controller is basically to generate the ON/OFF signals according to the fault current magnitude and to monitor the safe operation of the FCLID components. The controller employed in this work is designed such that the short-circuit current can be controlled in magnitude and for any period, determined by the FCLID component ratings. Only the current signal is required for the operation of the FCLID controller. Figure (5.4) shows the block diagram of the controller which consists of the following circuits:

- Current detector
- Precision full wave rectifier
- Discriminator
- Timing circuit
- Limiter circuit

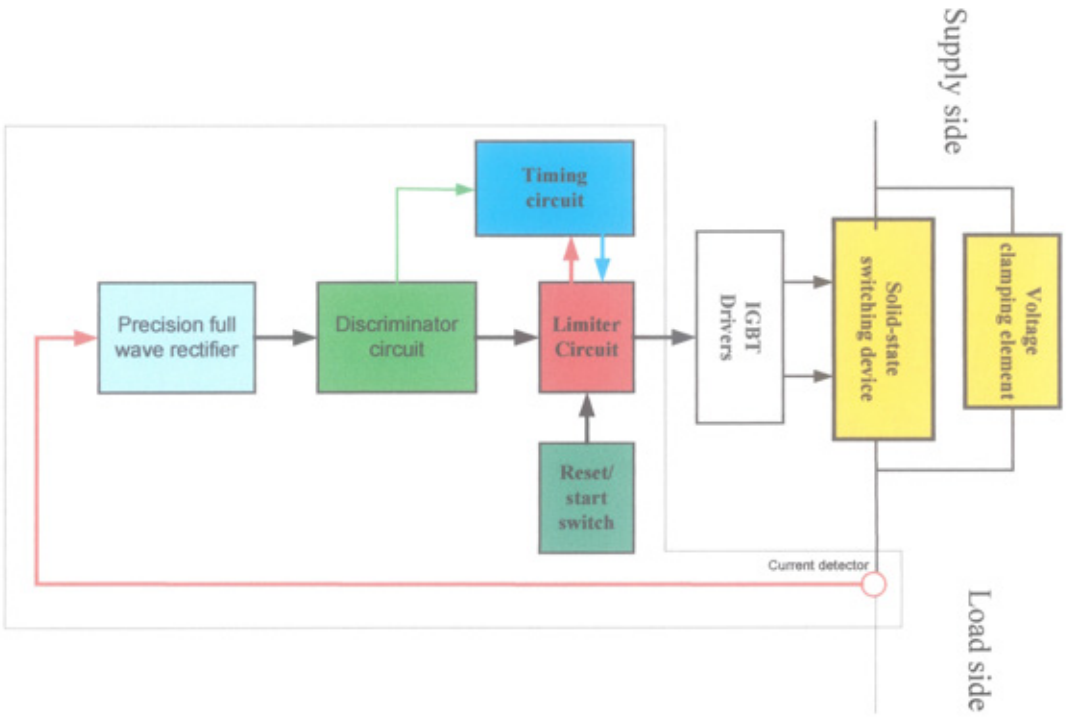


Figure 5.4 Block diagram of the FCLID controller

The controller is designed to switch on the IGBT continuously during normal operation. When the fault occur the current detector circuit send a feedback signal to the discrimination circuit. Based on the magnitude of the detecting current the discrimination circuit issues a control signal to switch the IGBT ON/OFF. The timing circuit is designed to switch off the IGBT completely and block the FCLID (in case of permanent fault) or to return the FCLID to the normal operation (in case of transient fault). The following sections describe the function of each circuit:

Current detector

The speed of the current detector is very important for the safe operation of the FCLID. The operation of this device is different than other devices mentioned in Chapter 1, in the detection of the fault current magnitude equal Imax, the device should be turned off instantly otherwise the current may exceed the maximum controllable turn off current of the switching devices. This requires continuous monitoring of the instantaneous value of the FCLID using a fast current detector. In this research a fast LEM current sensor with 500 ns response time is used.

Full wave rectifier

There are two types of the full wave rectification circuit the series cascade and parallel combination. The parallel circuit provide a very accurately sinusoidal wave to full wave rectification at unity gain and gives faster response as compared with the conventional series cascade rectifier. Figure (5.5) shows the test circuit for the parallel rectifier circuit. Figure (5.6) shows the current flow through the test circuit and Figure (5.7) shows the output of the parallel rectifier circuit.

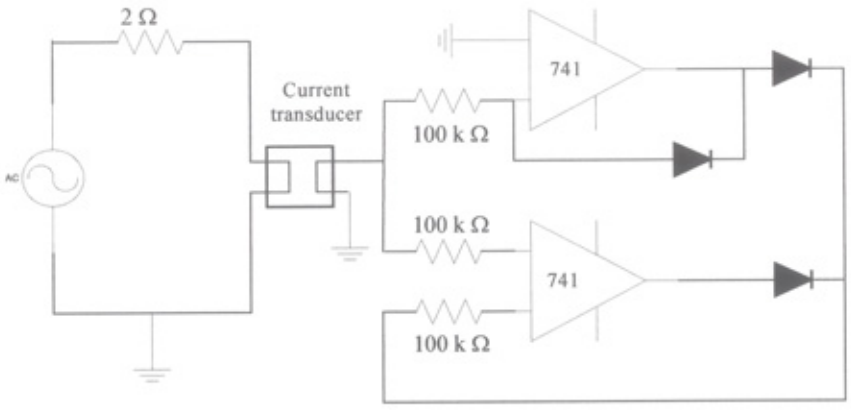


Figure 5.5 Test circuit of the full wave rectifier

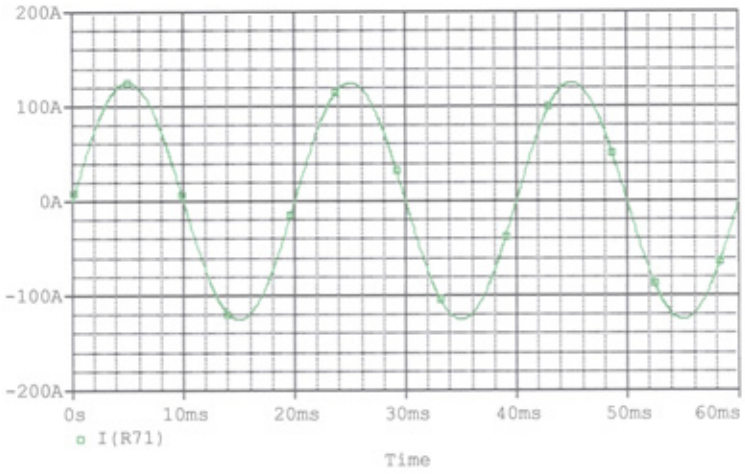


Figure 5.6 Measured current

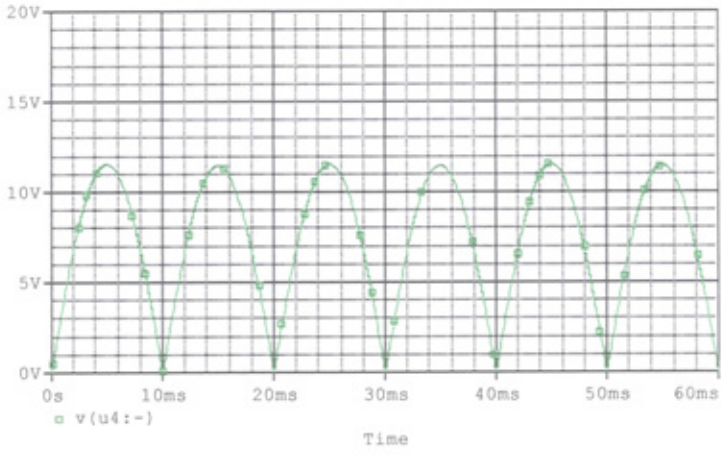


Figure 5.7 Output of the full wave rectifier circuit

Discriminator circuit

Figure (5.8) shows, the discriminator circuit which consists of three comparators; the first one (HI) for detecting Imax, the second one (LO) for detecting Imin and the third one for preventing malfunction (if Imin adjusted higher than Imax). Figure (5.9) shows the output of the rectifier circuit, LO comparator and HI comparator during normal operation. Figure (5.10) shows the output of the rectifier circuit, LO comparator and HI comparator during fault operation.

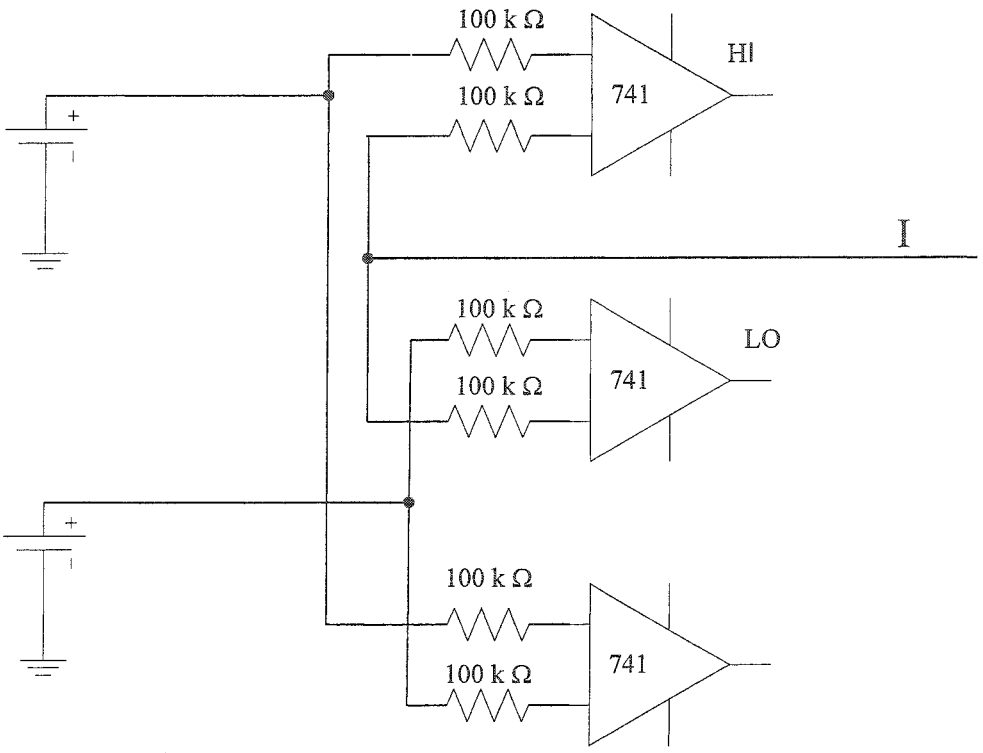


Figure 5.8 Discriminator circuit

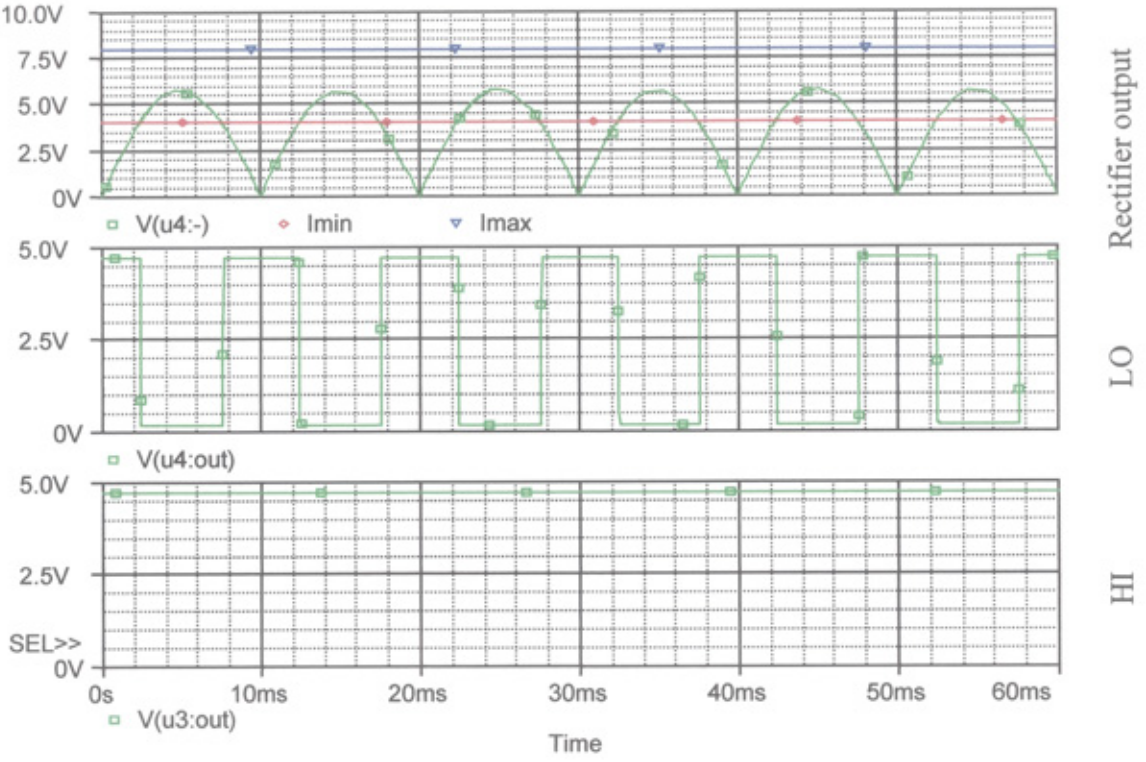


Figure 5.9 Output of the discriminator circuit (normal operation)

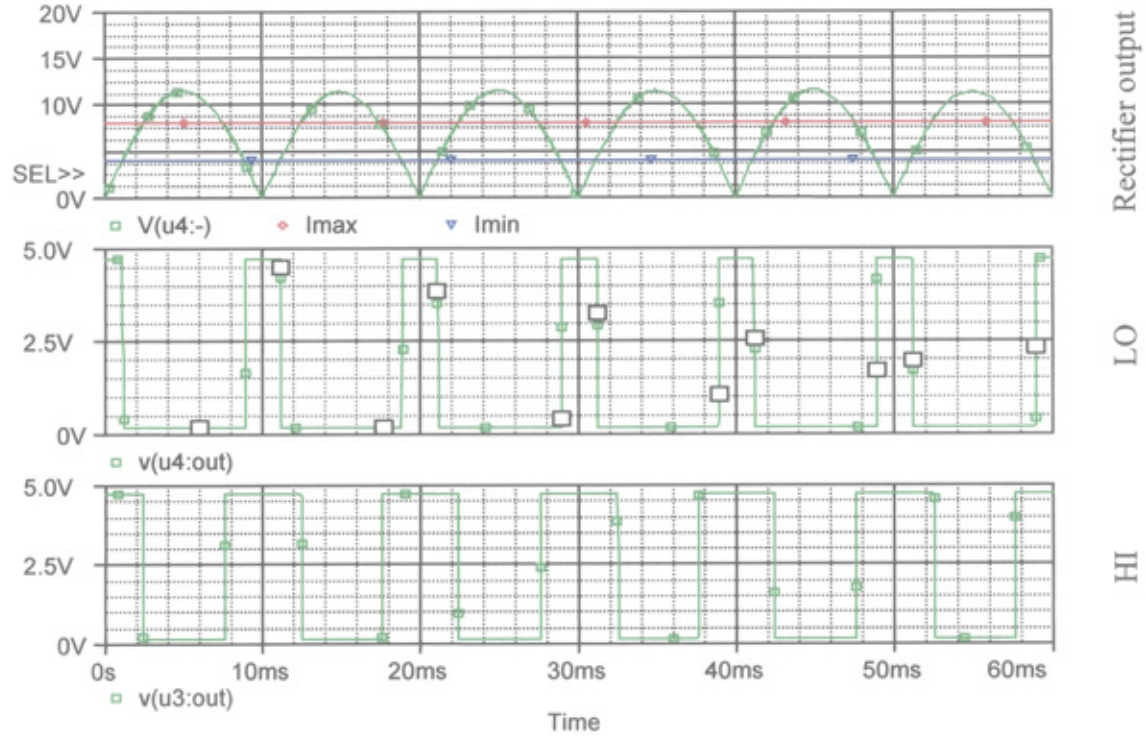


Figure 5.10 Output of the discriminator circuit (fault operation)

Timing circuit

The timing circuit is shown in Figure (5.11), it consists of two timers; a 555 timer (T1) and a retriggerable timer 74123 timer (T2) both timers are triggered by the limiter circuit. In case of a transient fault, the delay time generated by the 74123 is less than the 555 timer (FCLID operating time) and an ON/OFF signal is generated during the fault period. At the end of this period, both timers will automatically reset for the next operation and the FCLID return to the normal operation. In case of permanent fault the delay time of the 74123 is longer than the delay time of 555 and an interrupted commend is generated switch off the IGBT completely. In order to return to the normal operation the FCLID should be restarted manually.

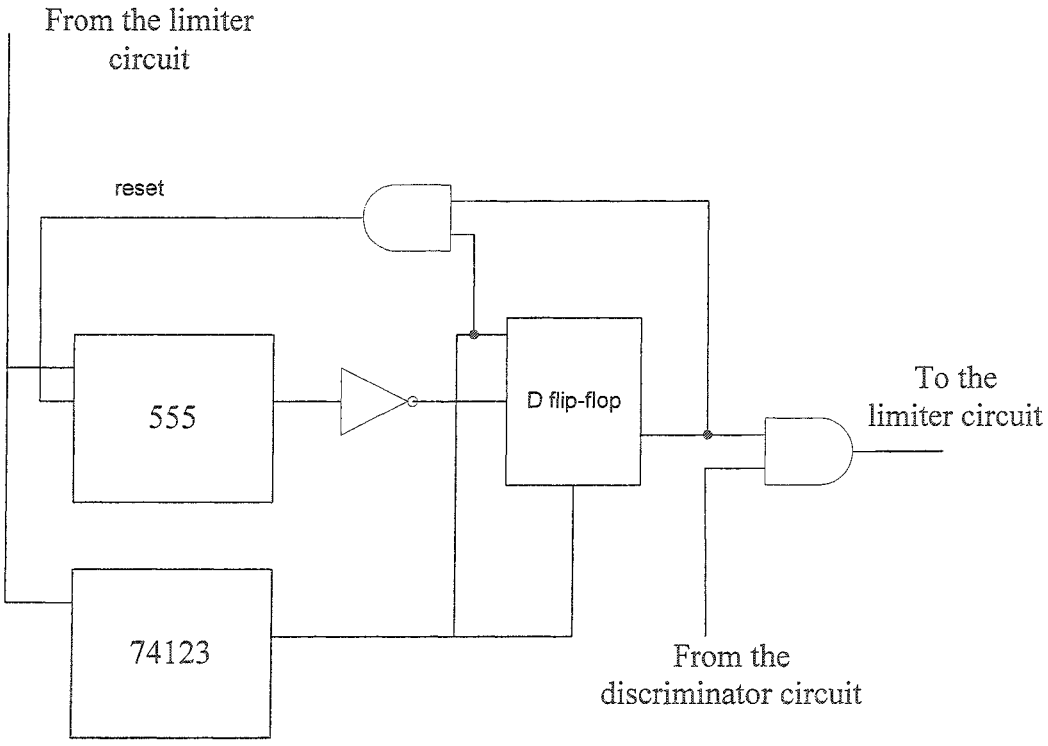


Figure 5.11 Timing circuit

Limiter circuit

Figure (5.12) shows the limiter circuit. This circuit takes the command from both the discriminator and timing circuits. During normal operation the output of the circuit is high turning the IGBTs ON. During a fault, the circuit produces a signal for the IGBT gate driver to switch ON/OFF the IGBT. At the end of the FCLID operating period, the IGBT is switched off completely and the fault current is permanently interrupted. At this stage the FCLID can be manually restarted by pressing the reset switch associated with the Imin comparator (in the discriminator circuit) to allow the FCLID back to normal operation again.

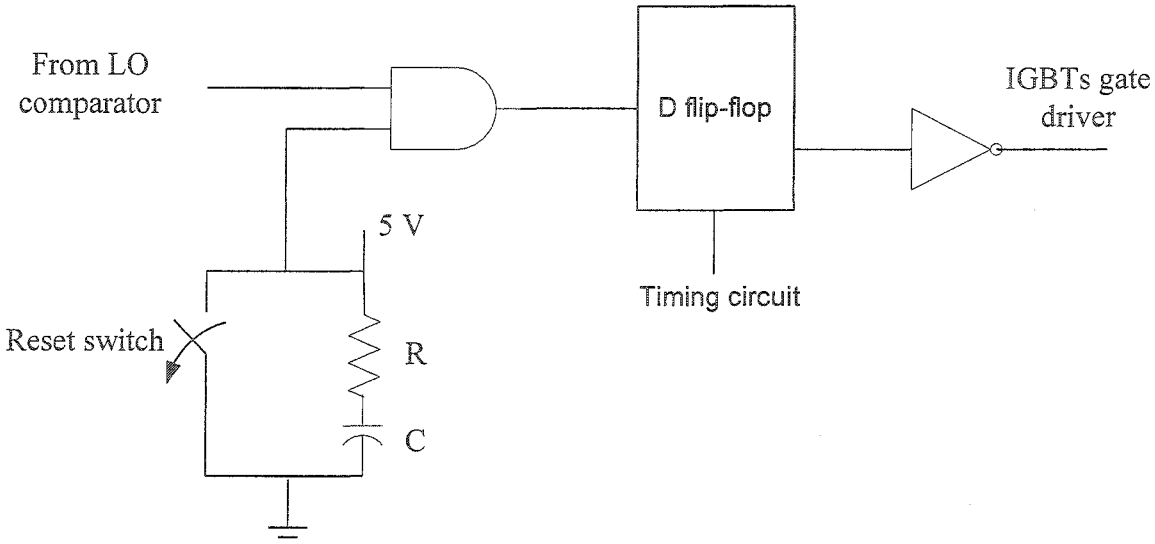


Figure 5.12 The limiter circuit

The complete circuit of the FCLID controller was simulated using ORCAD software package and is presented in APPENDIX C. In order to show the validity of the controller different simulation tests have been carried out under different condition. It is assumed that the pre-fault load current is less than 40 A and the prospective short-circuit current is

1 kA. Figure (5.13) shows the case where the current is limited to Imax = 120 A and Imin = 0 A.

Figure (5.14) presents the current waveform for the same case with Imin set to 30 A. Figure (5.15) illustrates the current waveform and the output of the HI & LO comparators and output of the timing circuit during permanent fault. Figure (5.16) gives the current waveform and the output of the timing circuit for a transient fault.

The simulation results confirm the validity of the proposed controller in performing the FCLID function under permanent and transient fault conditions. The complete circuit was assembled in one PC board as shown in Figure (5.17). Figure (5.18) demonstrates the functional block diagram of the whole controller of the FCLID including all indicators.

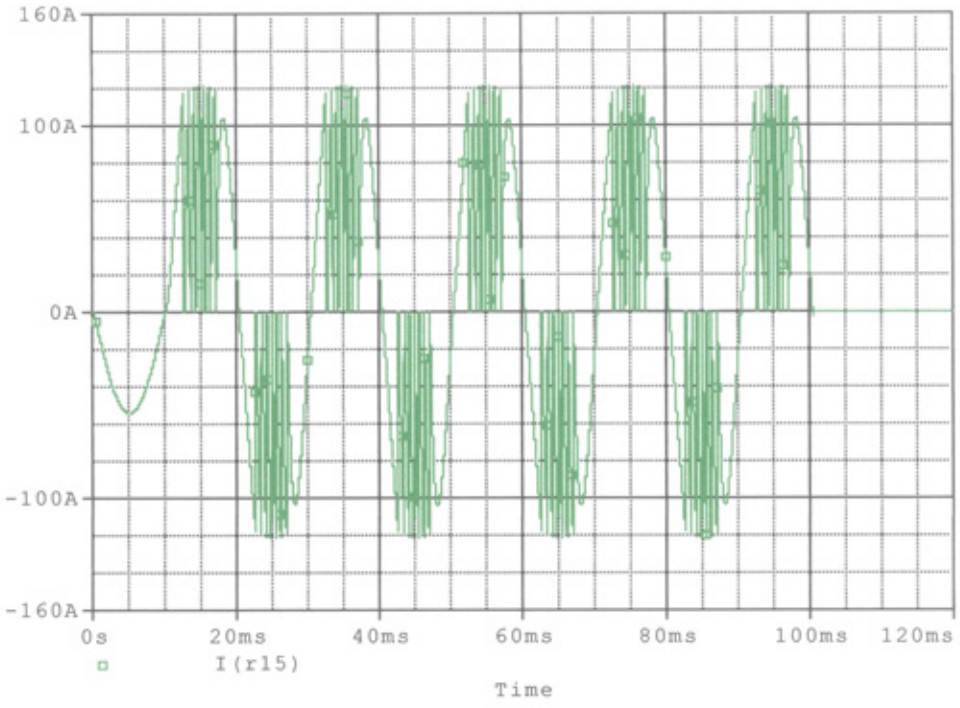


Figure 5.13 Current waveform for Imin = 0 A

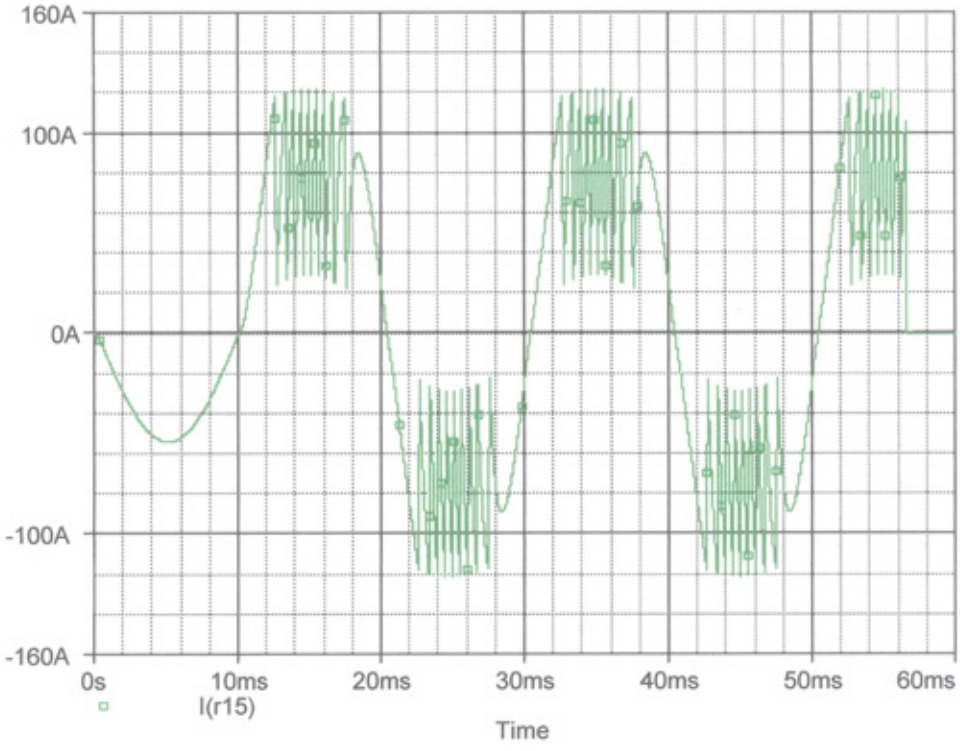


Figure 5.14 Current waveform for Imin = 30 A

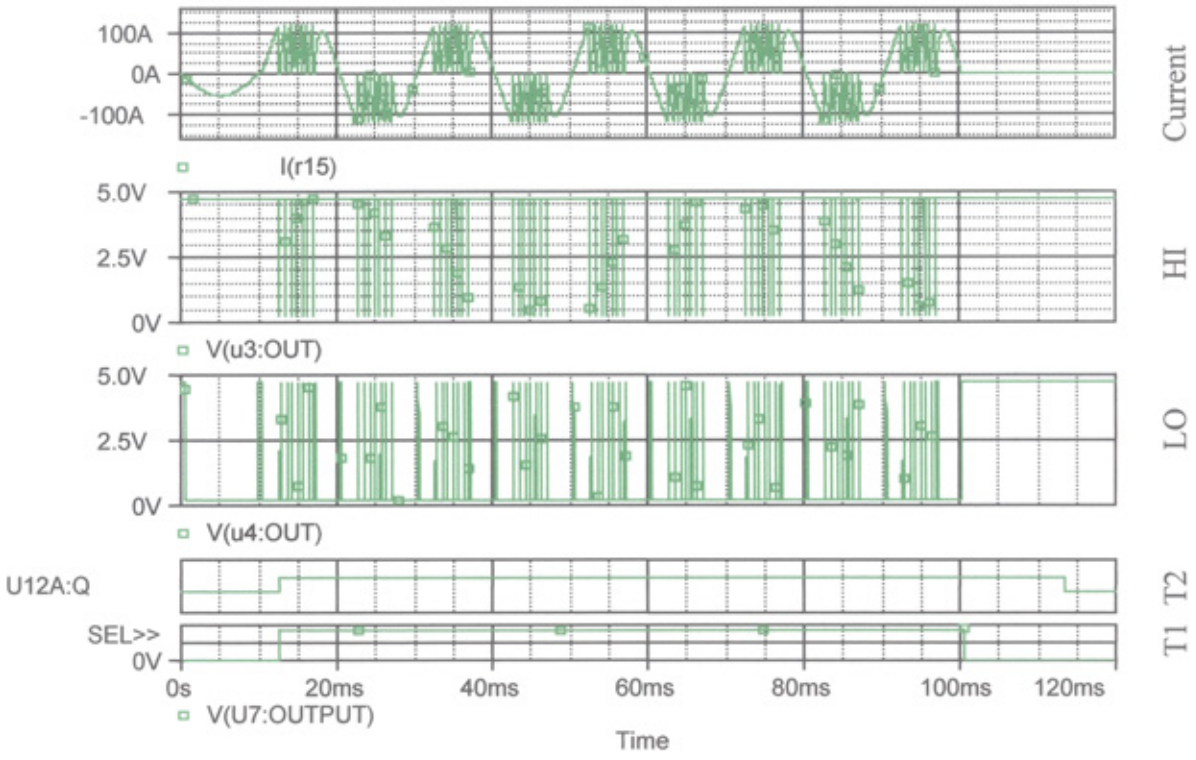


Figure 5.15 Current waveform and timing signals for a permanent fault

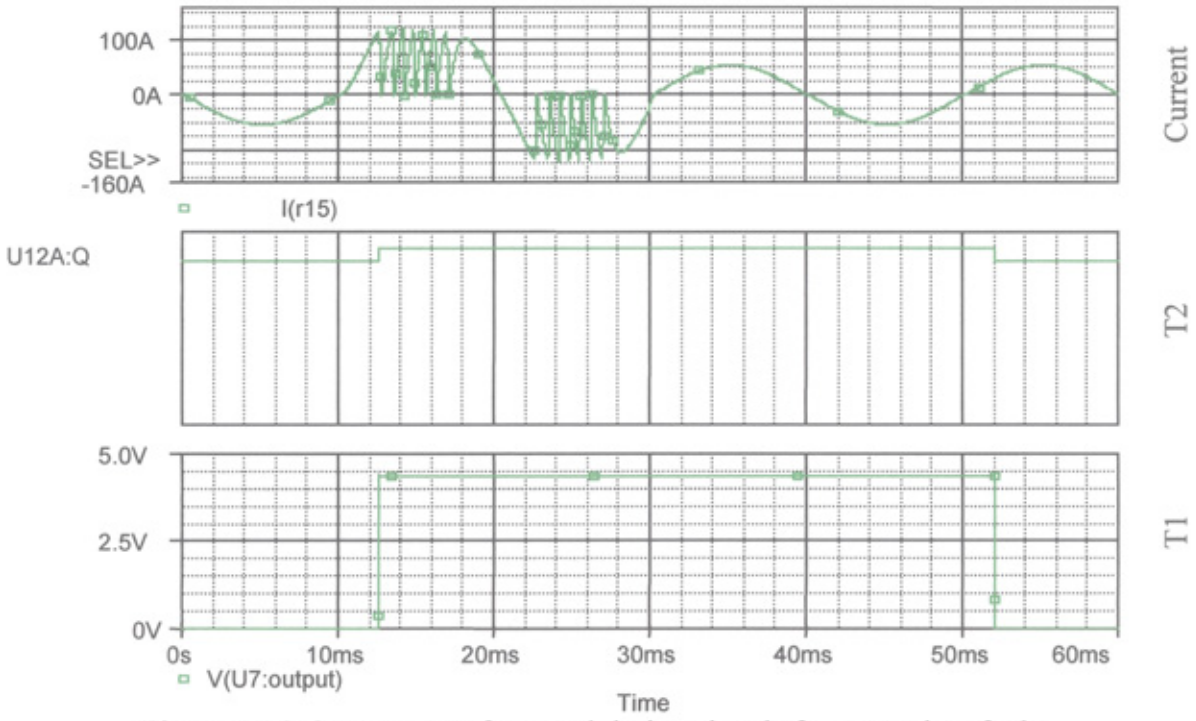


Figure 5.16 Current waveform and timing signals for a transient fault

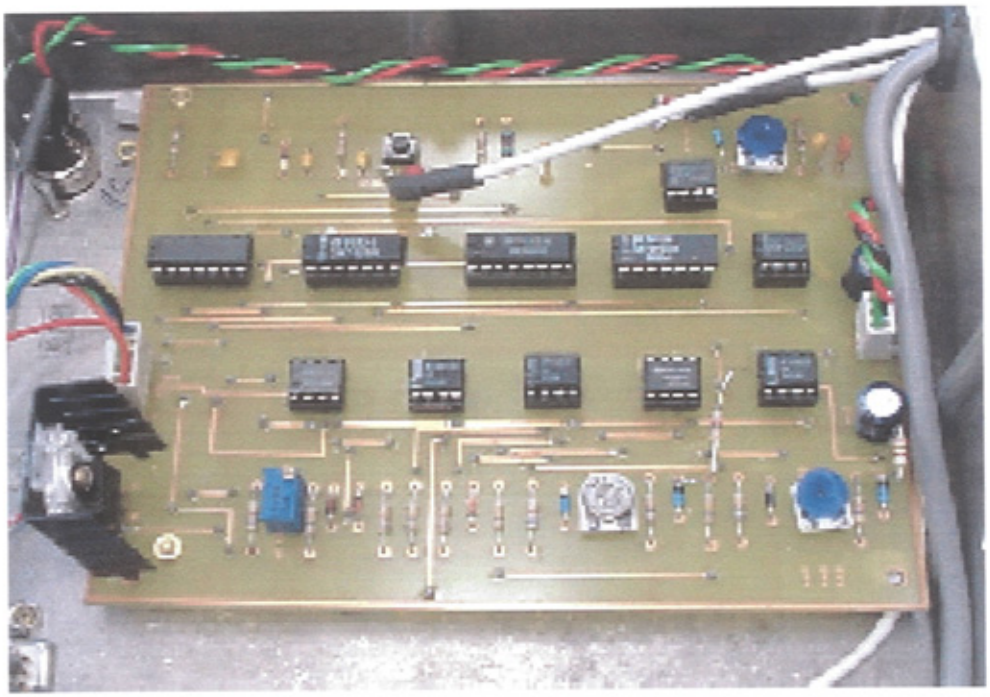


Figure 5.17 Controller of the FCLID

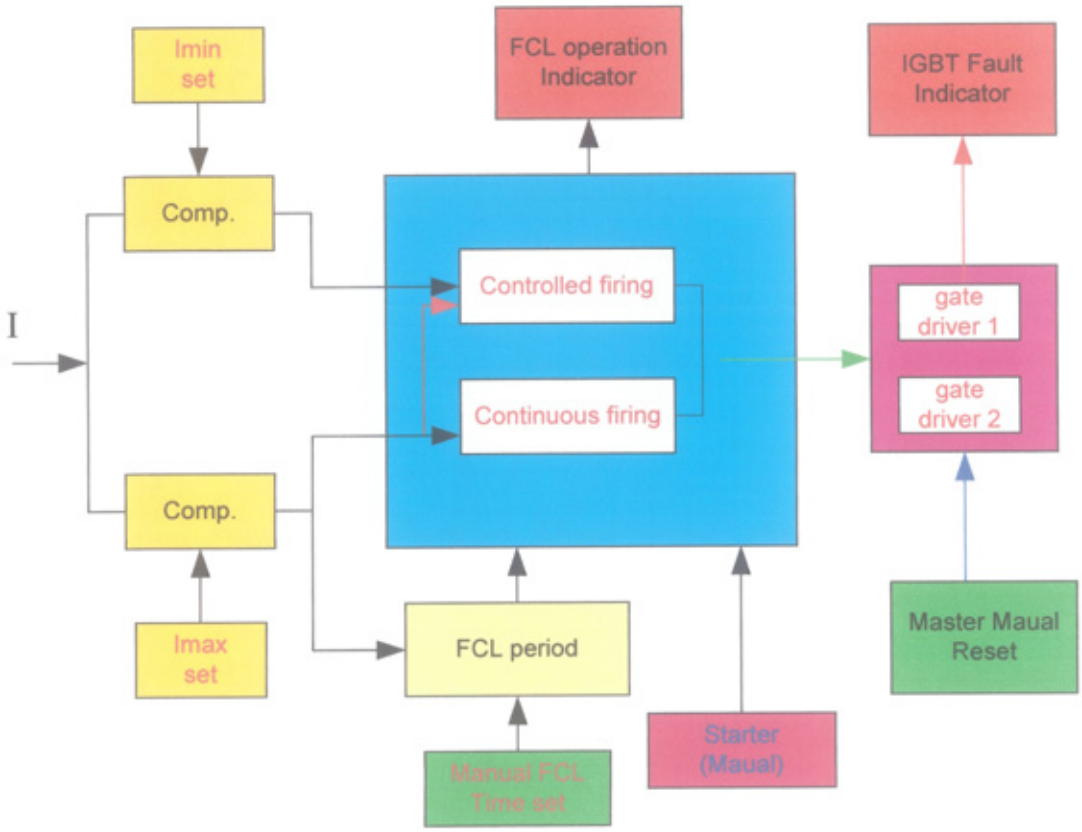


Figure 5.18 Functional block diagram of the whole controller of FCLID

5.3 Construction of The FCLID

Figure (5.19) shows the d.c. power supply used to drive the fans, current detector circuit, IGBT drivers and controller circuit. Figure (5.20) shows the IGBT switch and its snubber circuit which were fixed on the rear panel of the FCLID cabinet. Figure (5.21) shows both the controller and the IGBT drivers fitted in compartments in order to prevent RFI. It also shows the parallel combination of the varistors with the series resistors. Figure (5.22) shows the final product of the prototype FCLID. As can be seen, at the front panel there is one switch used to turn the FCLID ON/OFF and a reset switch to reset the control circuit components after the FCLID operation. Also, there are three indicators; the first one (above the reset switch) indicates the interruption of the current after the FCLID operation; the second and third indicators are for monitoring the IGBTs and their drivers. All the circuits have been constructed in a modular structure so that it is easy to maintain and service. The FCLID has been designed so that it can be used for further studies and analysis as well as for demonstration.

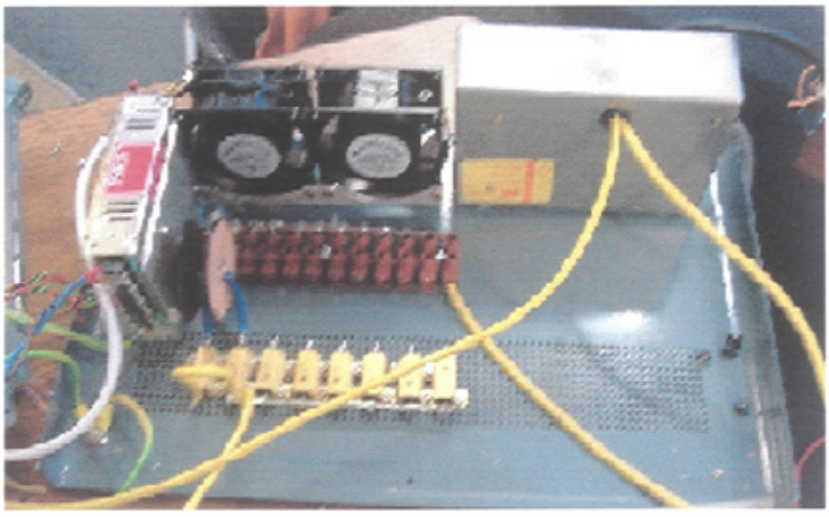


Figure 5.19 DC power supply and fans

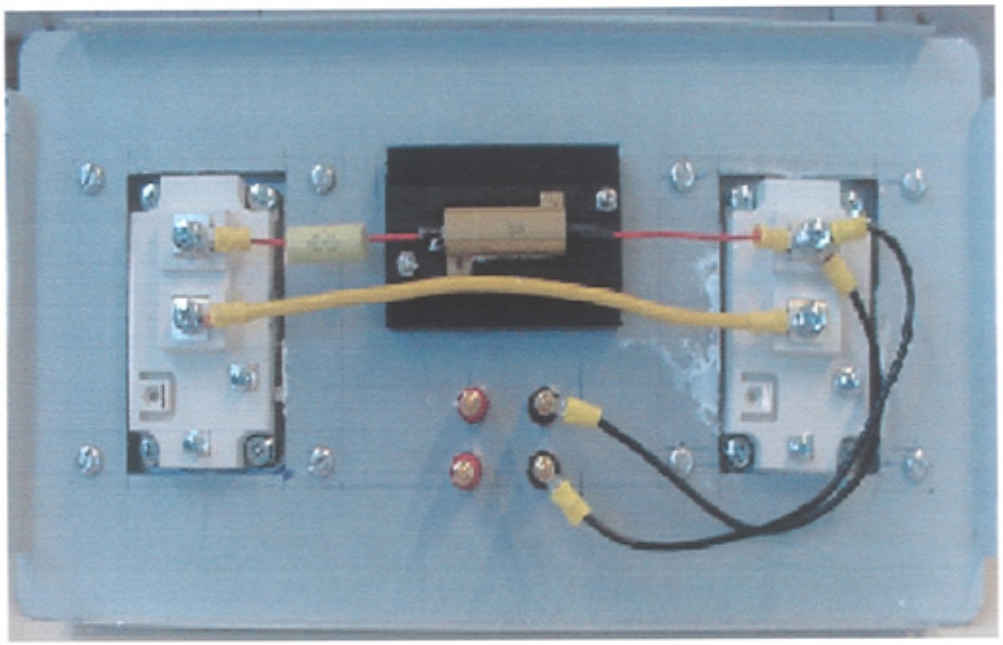


Figure 5.20 IGBTs and snubber circuit

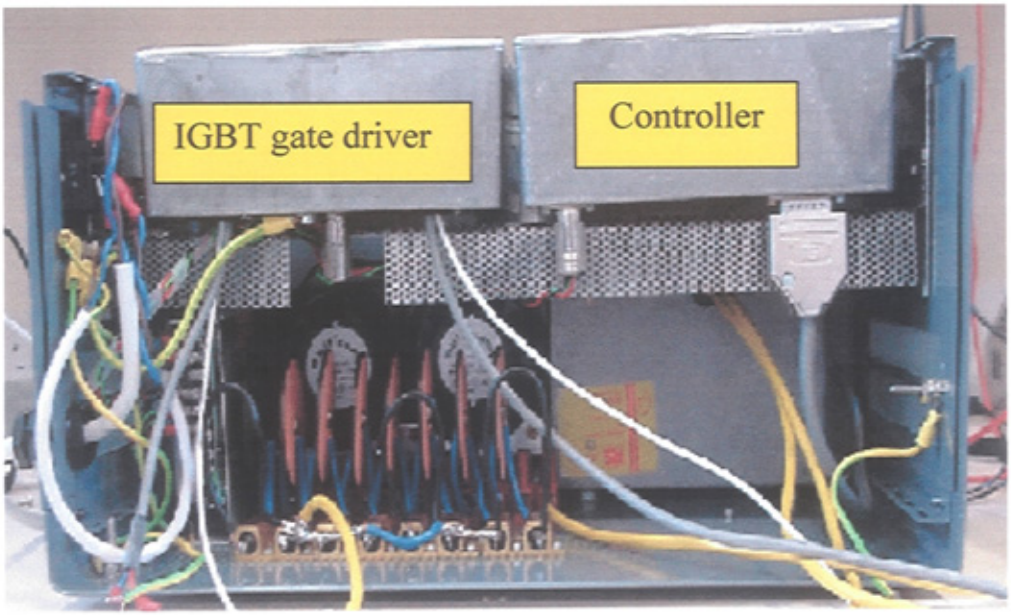


Figure 5.21 Varistors, IGBT driver and controller compartments

Figure 5.22 FCLID prototype

5.4 Measuring The Supply Short-Circuit Level

The FCLID has been designed to limit a short-circuit current of 1-2 kA to 120 A. So it is important to measure the short-circuit level of the supply in order to prevent damage of the FCLID due to high short-circuit level. Figure (5.23) shows the circuit arrangement used in this work to measure the short-circuit level. A high resistance, R and a.c. capacitor are supplied from the a.c. source. The resistance is inserted in series with the capacitor to limit the inrush current. A switch S is connected in parallel with the resistance R. When the switch S is closed, oscillation will result in a voltage across the capacitor, with a frequency f given as:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{5.4}$$

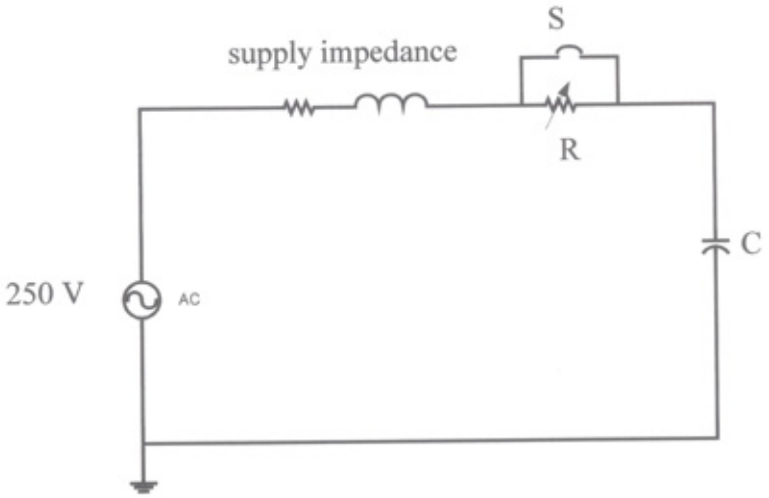


Figure 5.23 Test circuit

Two tests have been carried out to find the value of the supply inductance (the supply resistance is neglected). Figures 5.24 and 5.25 show the current waveforms when the values of the capacitors are 115 μF and 66 μF. The resonant frequencies from these results are 1785 and 2272 Hz which gives inductance values equal to 70 and 64.5 μH respectively. Therefore, the average short-circuit level at the supply point is approximately equal to 12 kA.

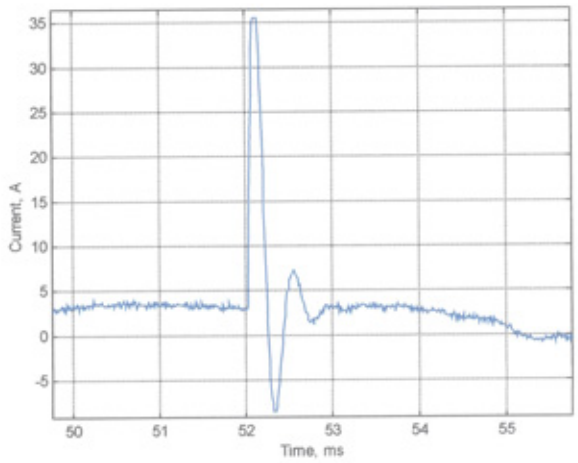


Figure 5.24 The current waveform (C = 66 μF)

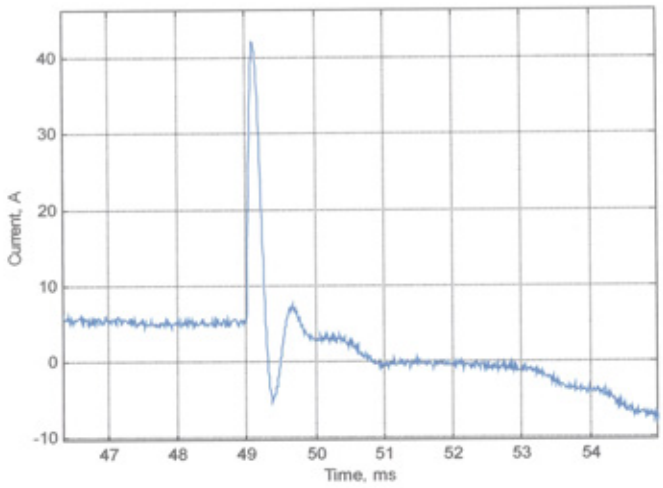


Figure 5.25 The current waveform (C = 115 μF)

The distribution transformer rating of the test circuit is 1000 MVA, its resistance and reactance per phase referred to 415 V are 0.00219 and 0.00863 Ω respectively [76]. The impedance between supply source and lower voltage busbars of primary substation equal to 0.0075 Ω. The calculated short-circuit level according to these parameter is 16 kA at the main circuit breaker. Comparing the measured short-circuit level 12 kA and the calculated short-circuit level at the circuit-breaker 16 kA, the reduction of short-circuit level is due to the cable impedance between the tested supply and main circuit breaker, also may be due changing the main supply source impedance. Therefore, in the lab set-up an impedance of 0.018 Ω, 0.63 mH was connected in series with the line to limit the level to 1 kA.

5.5 Experimental Set Up

Based on the analytical and simulation results, Table (5.1) summarises specifications of the FCLID prototype components. The solid-state switch was comprises two IGBTs with built in diodes, so that the switch can block high voltage in both directions. In addition a snubber circuit was connected across the switch to protect device from high (dv/dt)

during turn-off. Eight parallel varistors were connected in parallel to share the current when the solid-state switch is turned off. Figures 5.26 and 5.27 show a schematic diagram and a photograph of the test circuit, respectively.

To illustrate the performance of the FCLID prototype, an experimental test rig was set, as shown in Figure (5.28). Figures (5.29) shows the current and voltage waveforms when the pre-fault current was set to 18 A, fault angle $\alpha = 90^{o}$ and operating time = 0.8 s.

These results are in good agreement with the FCLID design specifications and it clearly show the ability of the FCLID to limit the fault current up to 0.8 s and then to interrupt it. Depending on the application, the operating time can be increased by increasing the number of IGBTs and varistors connected in parallel.

System / Device	Specification	Value	Units
Power system	Voltage level (L-G)	250	V
	Current	50	A
	Frequency	50	Hz
	Peak prospective short circuit fault current (per phase)	1	kA
Solid-state FCLID	Max. voltage	250	V
	Max switching current	120	A
	Max. operating time	0.8	s
Solid-state switch	Max rated voltage	1200	V
	Max pulsating current	400	A
	Max junction temperature	150	°C
	Total number of IGBT devices	2	
Snubber capacitor	Capacitance (C_s)	47	nF
	Peak voltage (V_{Cpk})	1	kV
Snubber resistor	Resistance (Rs)	15	Ω
	Power capability (Pmax @ 1 kHz switching frequency)	22	W
Varistor	Maximum clamping voltage	620	V
	Rated energy	880	J
	Number of varistors	8	

Table 5.1 Specifications of the FCLID prototype

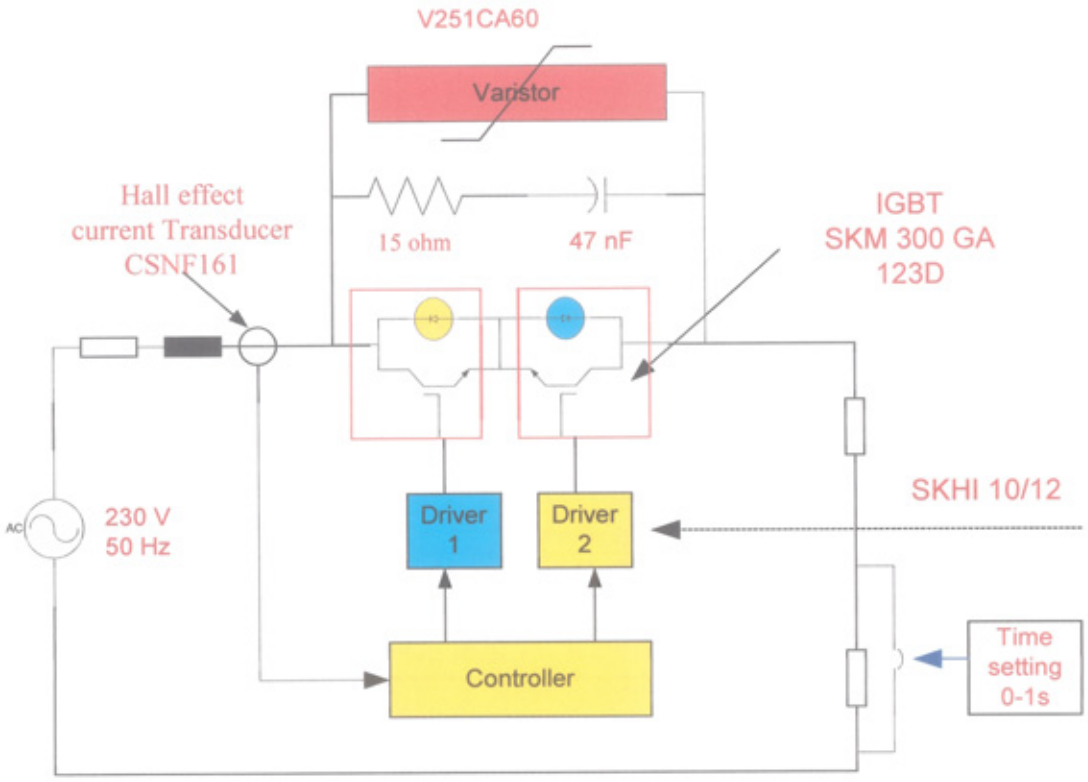


Figure 5.26 Schematic diagram of the test circuit

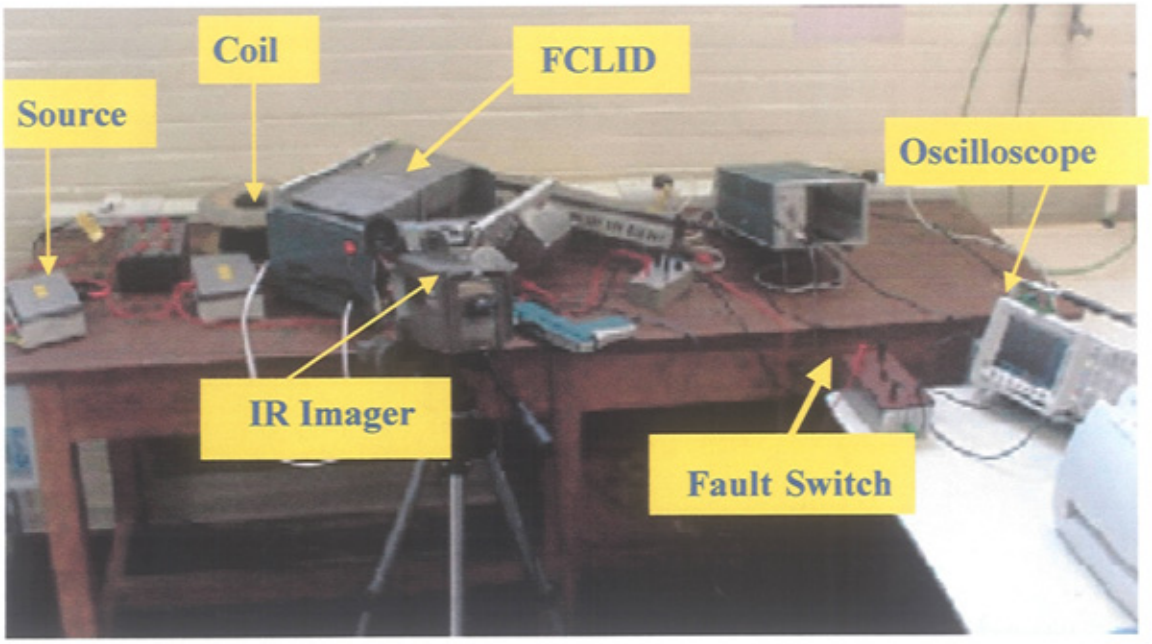


Figure 5.27 Experimental test circuit

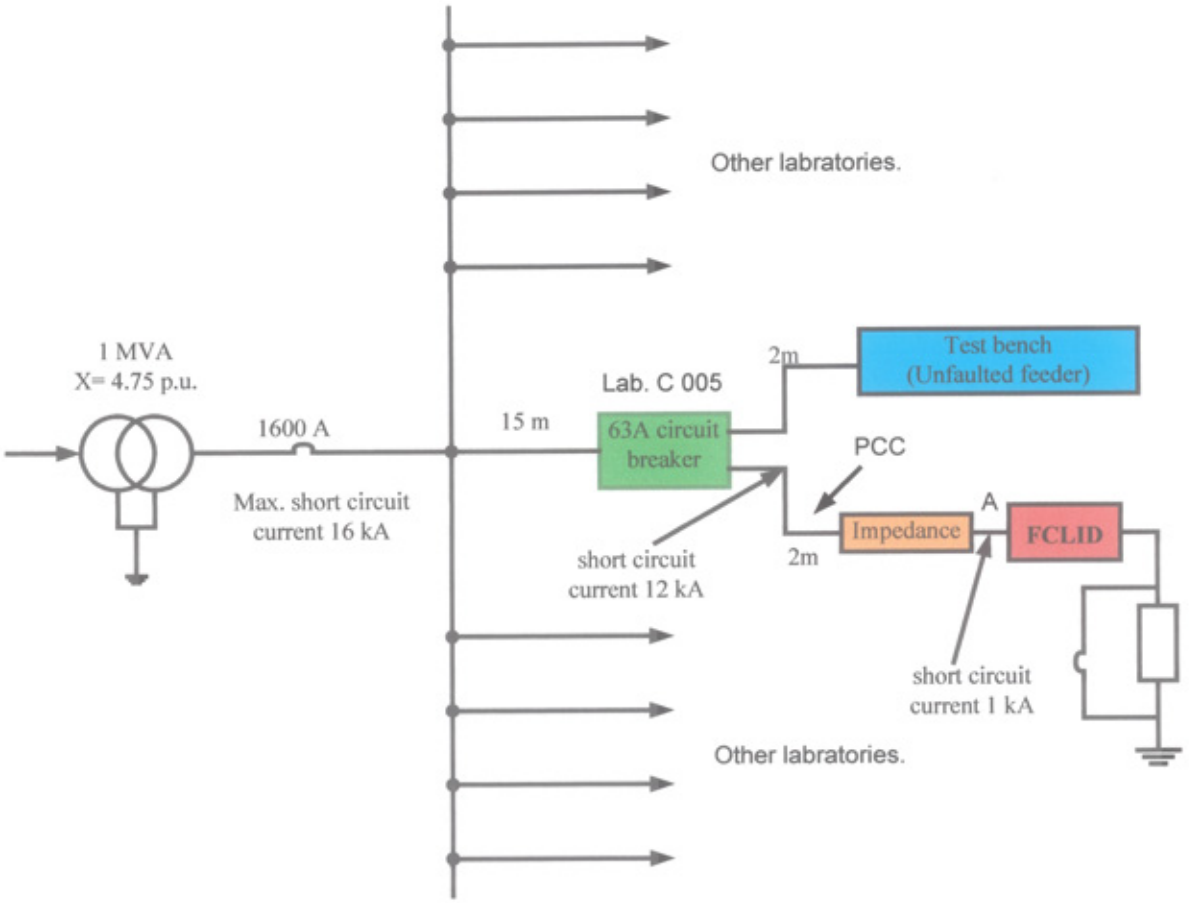
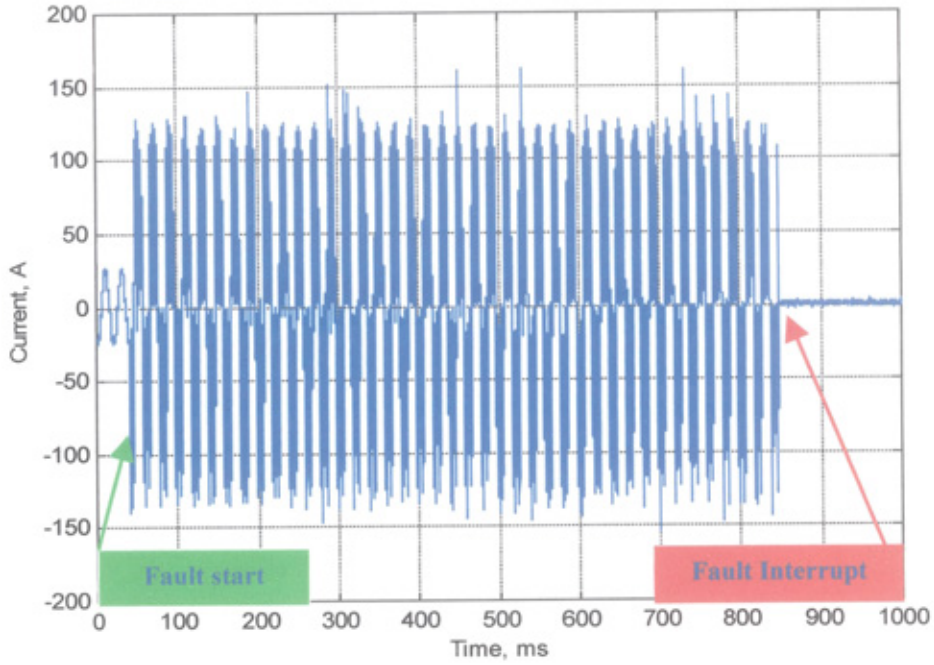
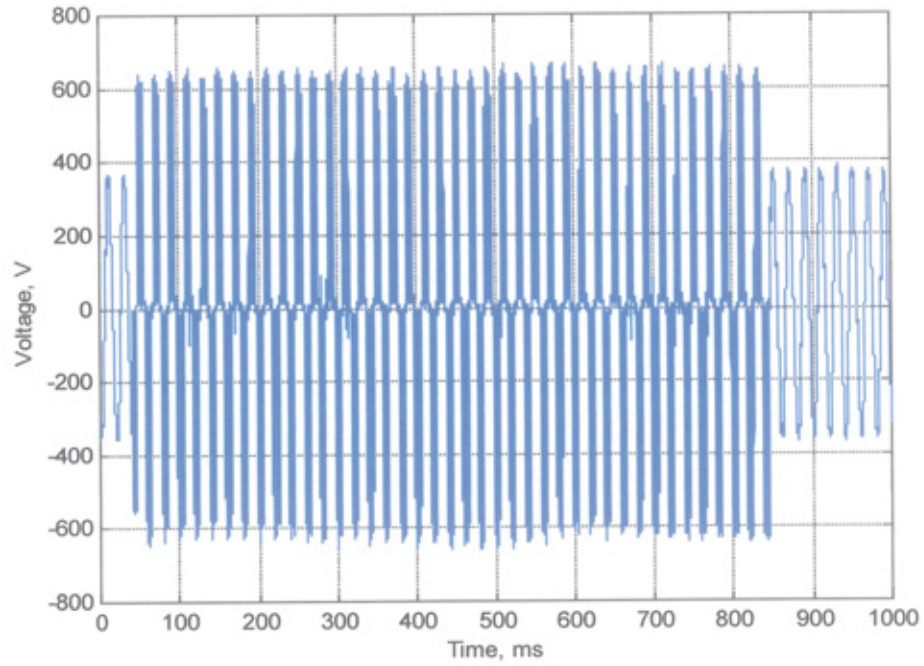


Figure 5.28 Typical tested distribution system



(a)



(b)

Figure 5.29 Current and voltage waveforms at A shown in figure 5.28

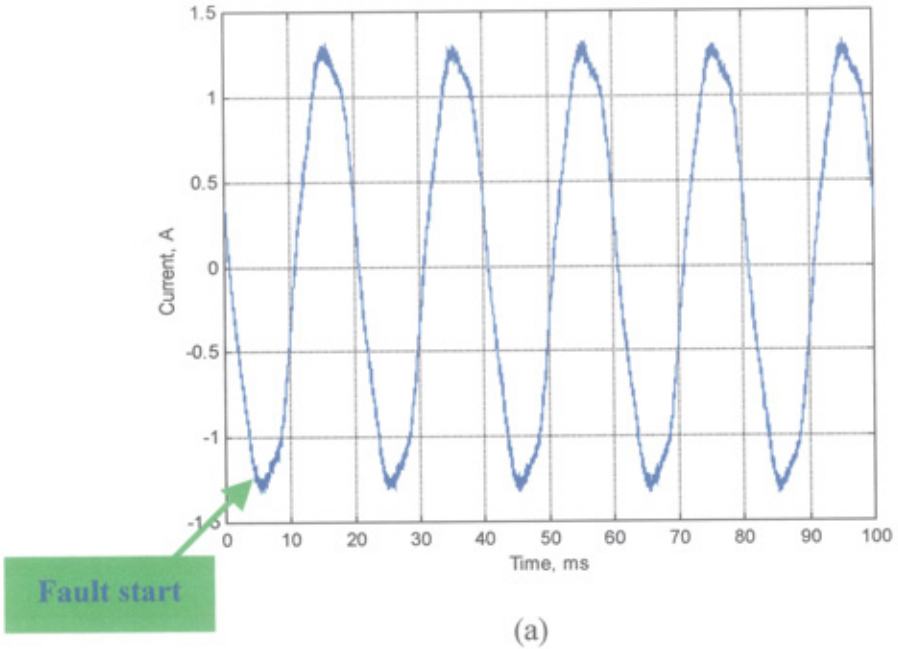
(I_{normal} = 18 A & $\alpha = 90^{o}$)

5.6 Effects of The FCLID on The Quality of Supply

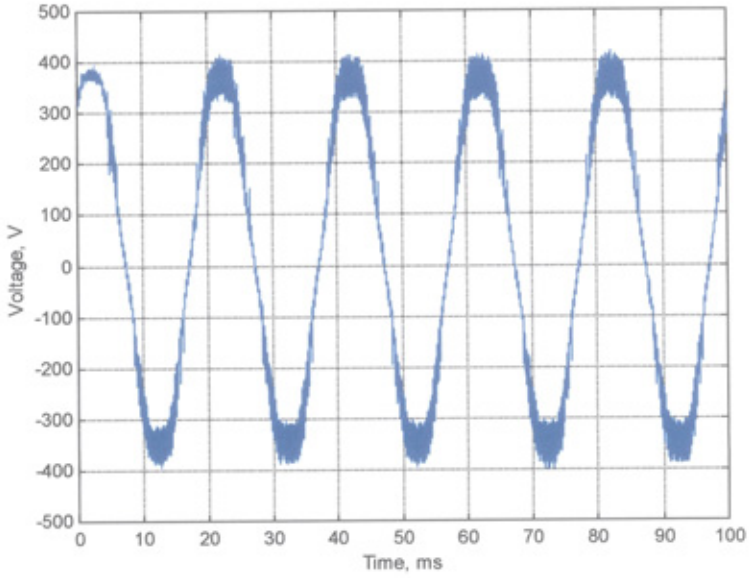
Various industrial equipment have different sensitivities to voltage sags. The main categories of sensitive loads are: motors, adjustable speed drives, discharge lamps and control devices. The consequences of voltage sag in the induction machine supply are speed loss and current & torque peaks that appear in the voltage drop and recovery points. These disturbances may trigger the motor or system protections.

In this work experimental tests were carried out on a single-phase 230 V, 1 kW, 1350 rpm induction motor to verify the simulation results from Chapter 2 (section 2.7). Figure (5.30) shows the motor current and voltage waveforms when the fault occurred near to the cable end (short-circuit current 1 kA). It can be seen that the FCLID is capable in mitigating the voltage sag without any change in both the motor speed (see Figure 5.31) and current.

The second test has been done when the fault occurs close to the FCLID. In this case the voltage at the point A (Figure 5.28) is determined by the varistor clamping voltage. Figure (5.31) shows the corresponding motor current, voltage and speed waveforms. It is clear from this figure that even if the fault is close to the FCLID, the latter is capable of maintaining the supply voltage close to its nominal value, thus preventing the motor speed from dropping.

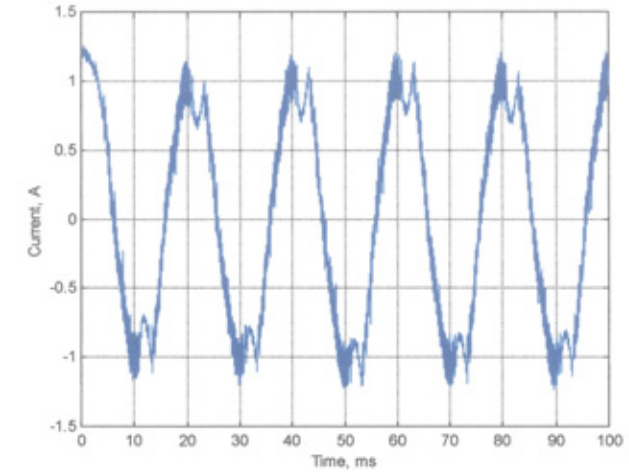


(a)

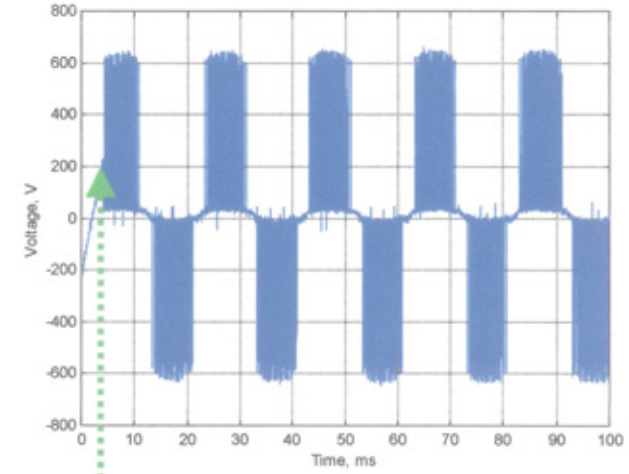


(b)

Figure 5.30 Motor current and voltage waveforms (fault close to the FCLID)

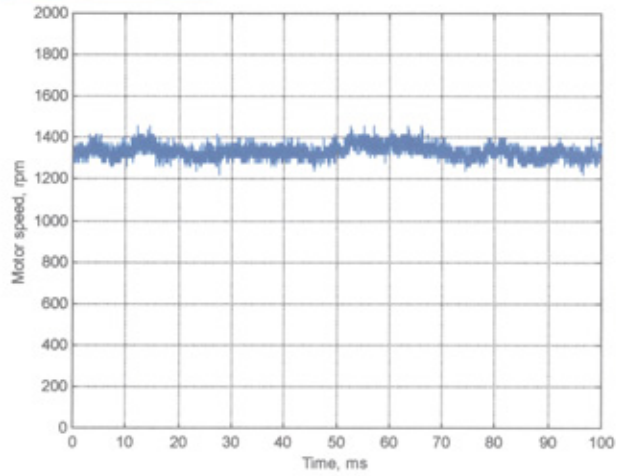


(a)



Fault start

(b)



(c)

Figure 5.31 Motor current, voltage and speed waveforms (fault close to the FCLID)

5.7 Practical Implementation of The FCLID

One practical implementation of the FCLID is the Hybrid Fault Current Limiting and Interrupting Device (HFCLID) with the following specifications (suitable for the NEDL network):

- Single-phase, 230 V and rated load current ≈ 400 A (r.m.s.)
- Prospective short-circuit current ≈ 5 kA (r.m.s.)
- Limited short-circuit current ≈ 1200 A (peak value)

The basic structure of the HFCLID is presented in the single-line diagram shown in Figure (5.32). As can be seen, the main components are a solid-state bi-directional switching device, a voltage-clamping element, an isolator, a vacuum circuit-breaker, a current sensor, a fault current detector & estimator, a switching pattern generator and over-temperature protection units. The circuit- breaker is connected in parallel with the switching device and is normally closed in order to reduce power losses during normal operation.

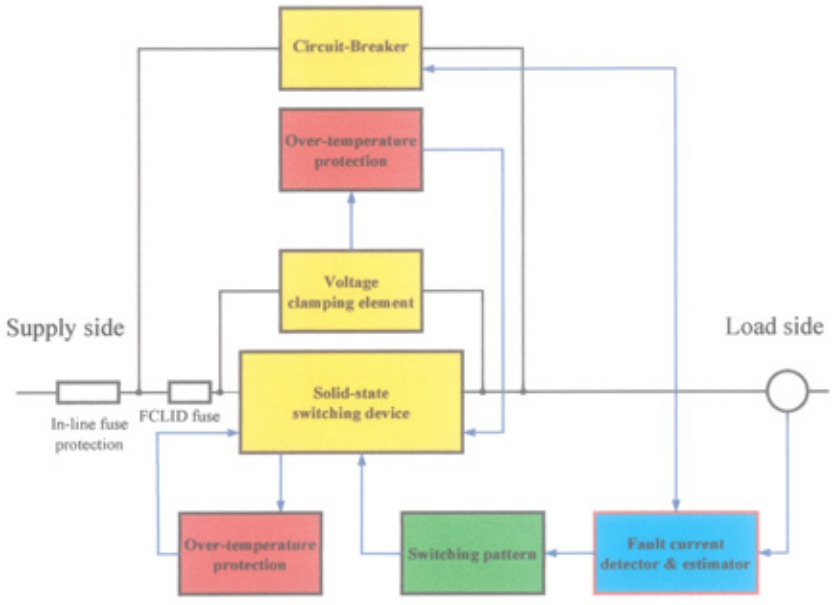


Figure 5.32 Block diagram of the HFCLID

Overheating of the switching device and the voltage-clamping element is prevented by 'indirectly' monitoring their temperatures using over-temperature protection units. A feedback signal to reset the controller is issued before the temperature limits (for the switching device and the voltage-clamping element) are exceeded.

Operation of the HFCLID

When a fault occurs, the circuit-breaker is opened and current interruption starts. The fault current is transferred to the switching device, which is instantly turned on after the first current zero crossing. The fault current now flows through the switching device and continues to increase. When the fault current exceeds a pre-set value (Imax), the switching device is turned off and the current is diverted to the varistor. Figure (5.33) shows the current before, during and after fault current occurrence. Figure (5.34) shows the current waveforms during the commutation period.

Modes of HFCLID operation

In order to achieve protection co-ordination, there are two modes for operating the HFCLID:

1- If the short-circuit level higher than 10 kA, the in-line fuse will rupture before the circuit-breaker can respond, as shown in Figure (5.35).

2- If the short-circuit level is less than 10 kA, two option may be adopted:

(i) When the fault is detected, the controller is set to open the circuit-breaker according to the fuse characteristic selected [77,78] and issue a signal to enable the FCLID operation. In this mode the device works under fixed values of Imax and Imin for any short-circuit level less than 10 kA and the total operating time is determined by the FCLID component ratings (maximum allowable temperature of devices).

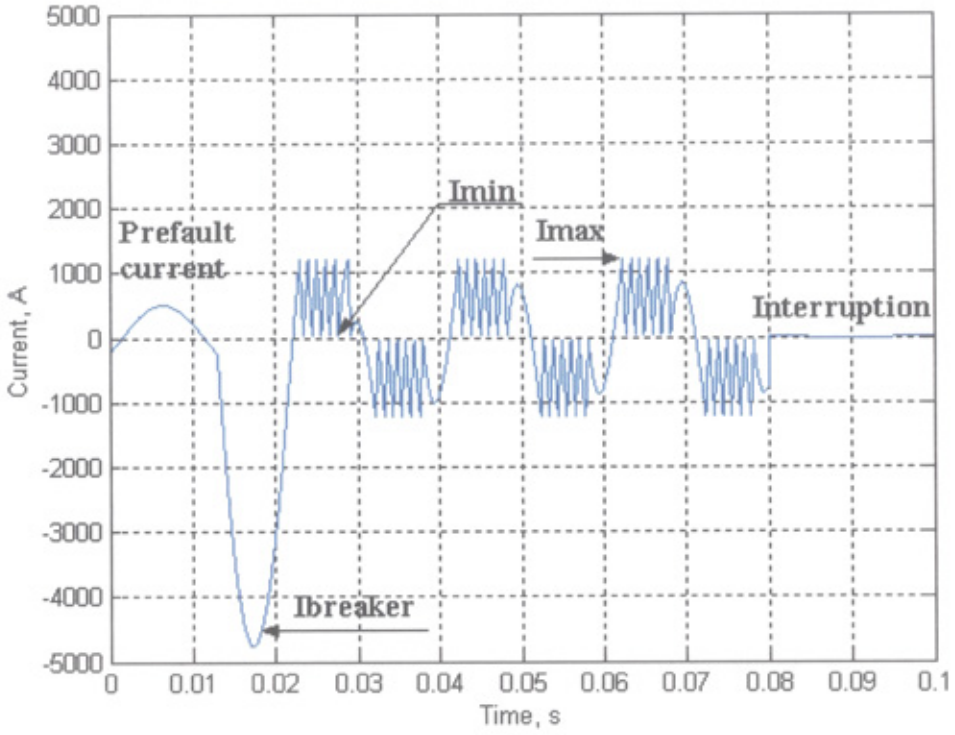


Figure 5.33 Current waveform

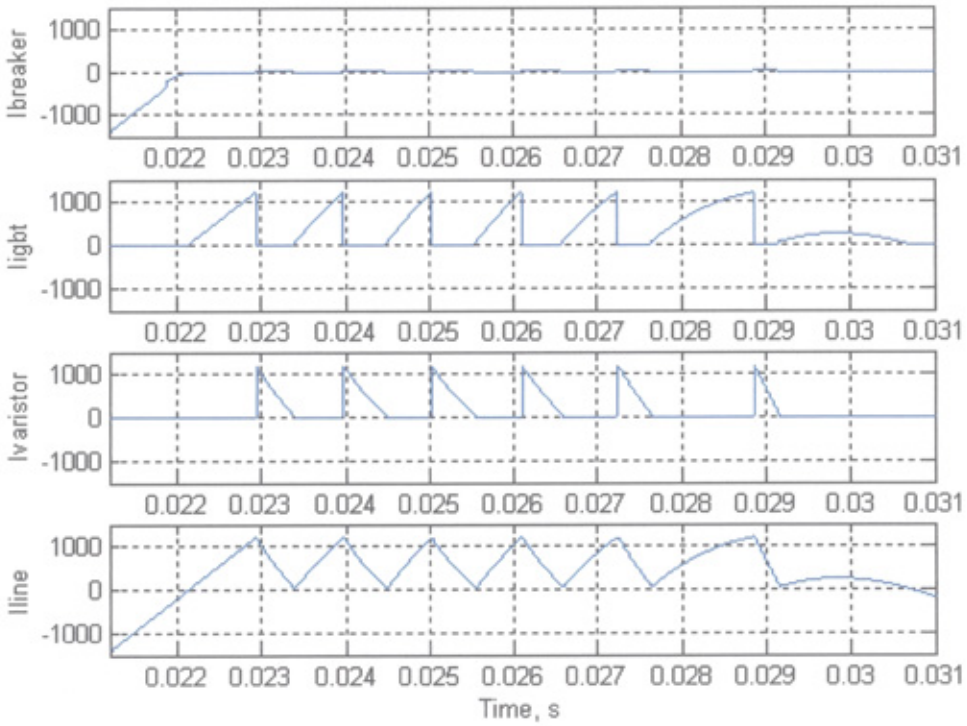


Figure 5.34 Current waveforms during the commutation period

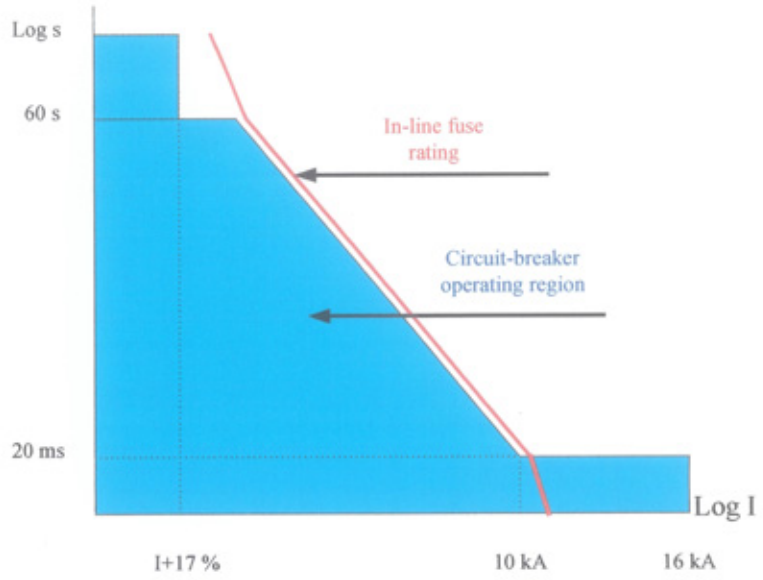


Figure 5.35 Circuit-breaker and in-line fuse characteristics

(ii) This option is based on estimating the short-circuit-level in the first peak after fault occurrence. If the short-circuit level is higher than 5 kA, the circuit-beaker is permanently opened and control signal to the FCLID is disabled. If the short-circuit level is ≤ 5 kA, the circuit-breaker is opened and FCLID operation is enabled. Based on the measured short-circuit level the FCLID operation may be controlled to suit the fault conditions (changing Imin, Imax and FCLID operating time).

The co-ordination between the in-line fuse and the circuit-breaker characteristics is achieved by setting the characteristics of the circuit-breaker lower than that of the in-line fuse. Figure (5.36) shows the characteristics of the in-line fuse (500 A), circuit-breaker (400 A) and the FCLID fuse (100 A). The FCLID is designed to limit the short-circuit level to 800 A (r.m.s.) for one second. Therefore, the FCLID fuse should be selected to withstand the limited current for a period higher than the FCLID operating time and capable to limit the short-circuit current before it reach its peak value in case of the FCLID failed as shown in Figure (5.36).

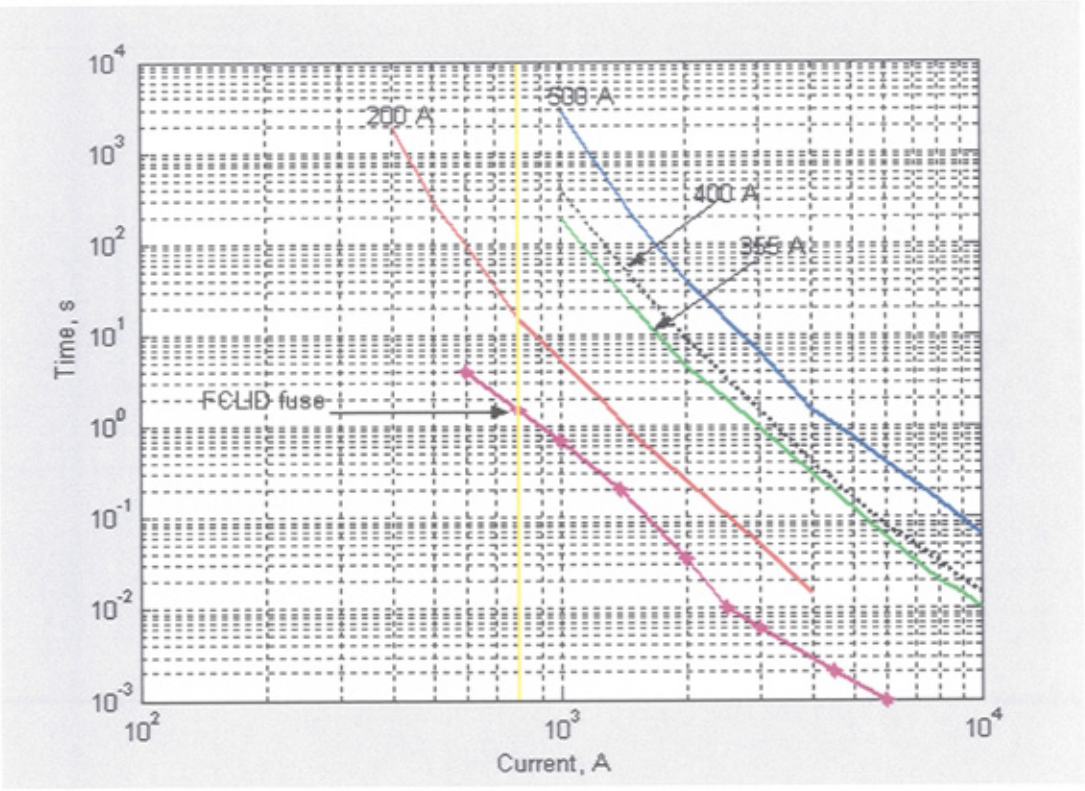


Figure 5.36 Characteristics of the fuse (Circuit-breaker, in-line and FCLID)

Based on estimating the fault current level, the HFCLID will operate for all short-circuit level less than 10 kA, if the short-circuit level higher ≥ 10 kA the in-line fuse protection will operate.

Figure (5.37) shows a block diagram of the suggested hybrid controller. The controller comprises two parts; one is analogue and the other is digital (micro-controller or microprocessor). Based on the feedback information from the digital part, the analogue controller sets the maximum & minimum currents for the switching process during the FCLID operation and interrupts the fault current completely when the maximum operating time of the FCLID or maximum temperature of the devices are reached.

The digital controller performs three functions:

First, it estimates the short-circuit level in the first peak after the fault occurrence and defines the mode of operation of the HFCLID. Based on the estimated fault current, it allows the maximum and minimum values of current to be adopted to suit the system requirement. By controlling the minimum and maximum current levels, the limited fault current level can be controlled to a desired level, which provide co-ordination with the other protection devices.

Second, it predicts the junction temperature of the solid-state device, as described in section 3.4. Based on the predicted temperature, the digital controller adjust the FCLID parameters to suit the system requirements (improving harmonics, adjusting short-circuit level, etc.) and issue a trip signal to permanently interrupt the current before reaching the maximum allowable junction temperature.

Third, it predicts the varistors temperature as described in section 4.10. Based on the calculated temperature the operating time of the FCLID is predicted and the controller determines the instant that the device should be turned off permanently before exceeding the thermal stability limit of the varistors (maximum energy handling capability). Implementation of this controller can lead to an adaptive and fail-safe FCLID.

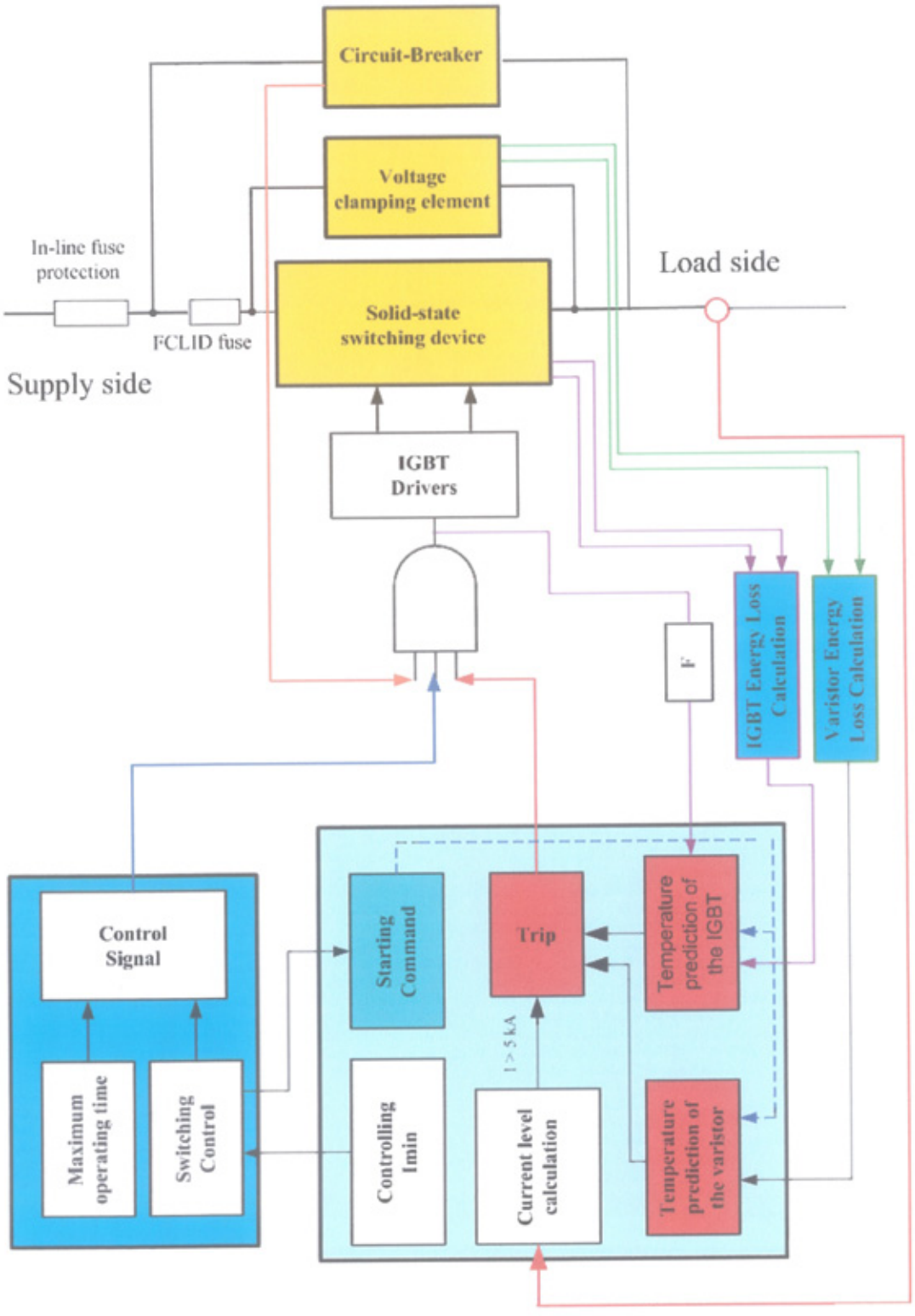


Figure 5.34 Intelligent controller of the HFCLID

5.8 Design Specifications of The 11 kV FCLID

For a three-phase 11 kV industrial networks, typical operating requirements suggest a 2.5 p.u. overvoltage withstand, giving a maximum operating phase voltage of 15.9 kV. The maximum allowable voltage withstand of an IGBT is 3.3 kV, so five IGBT pairs per phase can withstand 16.5 kV. For safety reasons, a redundancy of single IGBT pair is added to each phase of the system, this provides a voltage withstand of 19.8 kV. The total number of IGBTs required is 12 per phase, including antiparallel diodes as shown in Figure (5.38). This may seem costly, but security is very important. The reduced voltage stress on the IGBTs will allow them to work for longer period, since they are not operating close to their maximum rating. Based on the theoretical, simulations and experimental works on the prototype FCLID the preliminary outline design specification of a solid-state FCLID suitable for 11 kV distribution is presented in Table (5.2).

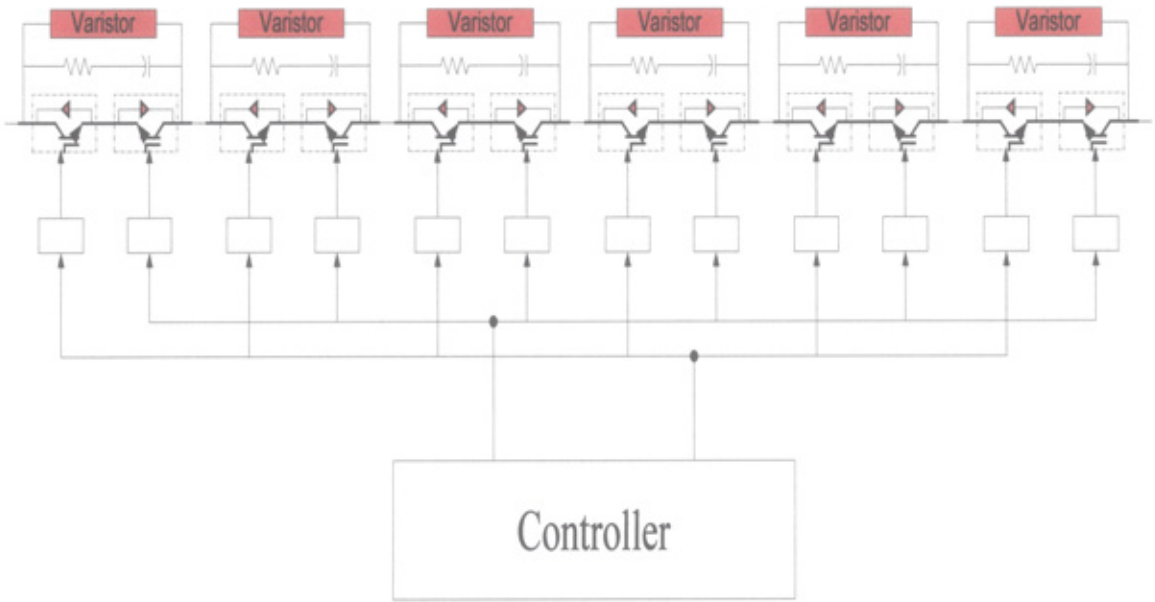


Figure 5.38 The 11 kV FCLID: series connection of AC switches

System / Device	Specification	Value	Units
Power system	Voltage level (L-L)	11	kV
	Current	600	A
	Frequency	50	Hz
	Peak prospective short circuit fault current (per phase)	15	kA
Solid-state FCLID	Max. voltage	19.8	kV
	Max switching current	1500	A
Solid-state switch	Max rated voltage	3.3	kV
	Max pulsating current	2.4	kA
	Max junction temperature	150	C^o
	Total number of IGBT devices per phase	12	
Snubber capacitor per 1 IGBT	Capacitance (C_s)	1.5	μF
	Peak voltage (V_{Cpk})	4	kV
Snubber resistor	Resistance (Rs)	5	Ω
	Power capability (Pmax @ 1 kHz switching frequency)	2000	W
Varistor	Maximum clamping voltage	3	kV
	Rated energy/ 10 cycle	250	kJ

Table 5.2 Design specifications of 11 kV FCLID

5.9 Conclusions

The design and successful development of the 230 V FCLID prototype have been presented. The experimental results presented in this chapter provide a fair validation for the computer simulation results. There is agreement with the simulation results and design specifications on the controllability of the short-circuit current under different conditions. Based on the analysis, simulation and experimental tests, the following can be concluded:

- This FCLID is able to successfully limit a potential short-circuit current of 1 kA (r.m.s.) to 120 A (peak). The FCLID responds within a 1 μs delay after fault occurrence.
- The proposed method for improving the current sharing between parallel varistors has shown to be successful.
- The FCLID prototype is capable of limiting the fault current for up to .8 s, so that co-ordination with other protection devices can be achieved.
- The developed prototype can be used for further work to develop a suitable device for higher voltage and current levels where more application can be found.
- HFCLID is a practical implementation of the FCLID combining solid-state switches and vacuum circuit breaker. The design analysis confirm the capability of this device to limit and interrupt short-circuit levels to any desired level (by controlling Imax & Imin) for relatively long period. This can assist in setting protection co-ordination within the distribution network and to locate the fault position. The suggested controller allows the HFCLID to adopt its parameters to suit the requirements of the power system networks.

CHAPTER SIX

HARMONICS ANALYSIS AND PERFORMANCE IMPROVEMENT OF THE FCLID

6.1 Introduction

Power system harmonics have been a growing concern for power engineers in the last decade because of the rising number of power electronic devices used in power networks [79]. These devices may not only increase the power losses of the electrical and electronic equipment, but also cause the fail or misoperation or shut down of other equipment [80]. In addition, the harmonic resonance can also cause serious problems such as overvoltages in the power system which may damage the power factor correction capacitors [81,82]. These effects can be costly to the utilities and customers due to the production downtime and equipment failure. Therefore it is extremely important to perform the harmonic flow analysis for FCLIDs within the power system before installing them in a real distribution network.

IN THIS CHAPTER, the harmonics caused by the fault current limiter are analysed and a MATLAB/SIMULINK model was designed and built to analyse the harmonic level. The calculated harmonics are checked against IEEE standard 519-1992 [83] and the UK standard G5/3 [84], regarding short duration harmonics. A control method is proposed to improve the harmonic signature. Laboratory experiments are performed to verify the harmonic calculation and the control method. Tests are also carried out to investigate the risk and solutions regarding harmonic resonance with power factor correction capacitors

in the network or cable capacitance. The effect on sensitive loads such as switching mode power supplies in the customer loads is also investigated.

6.2 Harmonic Analysis and Improvement

The Fast Fourier Transform (FFT) Technique is a very effective tool for performing a spectrum analysis that permits the calculation of the harmonic components. The PSB provide an excellent FFT Block for the Fourier analysis of the input signal over a running window of one cycle of the fundamental frequency. First and second outputs return respectively the magnitude and phase (degrees) of the harmonic component specified. In this study only the magnitude of the individual harmonics has been selected.

Figure (6.1) shows the frequency spectrum of the current waveform shown in Figure (2.6 a). In deriving the spectrum, the current was sampled for one fundamental cycle and Fourier analysis was then applied to the sample. It is observed that the harmonics originate from two distinct mechanisms: the harmonics around the average switching frequency of the semiconductor devices in the FCLID, and the lower order harmonics due to the constant Imax and Imin modulation control. The latter have similar distribution to the harmonics in a square wave [79].

Referring to Figure (2.4), the simulated voltage waveforms across the FCLID and at the PCC are shown in Figure (6.2). During operation, the FCLID alternatively presents the clamping voltage of the varistor (varistor conducting) and about 0 V (switch turned on) in series in the power circuit. The voltage across the FCLID (upper trace) is therefore very distorted.

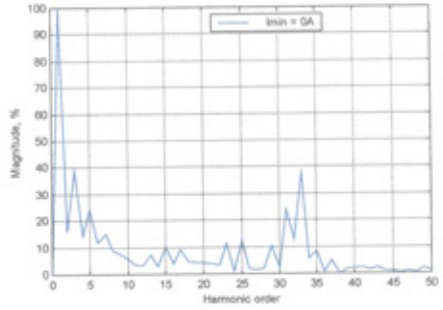


Figure 6.1 Frequency spectrum of the FCLID current

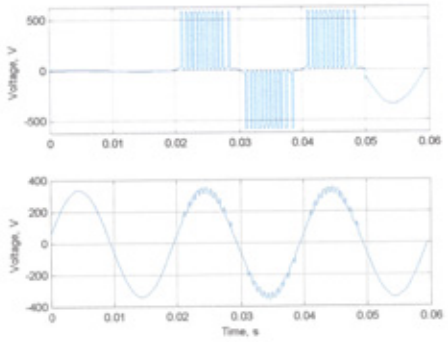


Figure 6.2 Voltage waveforms across the FCLID and at the PCC

As for the voltage at the point of common coupling, the harmonics in the FCLID voltage are divided between source impedance and the impedance from the point of common coupling to the fault. Therefore, as long as the FCLID is installed close to a strong supply and the fault location is sufficiently far from the FCLID, the voltage at the point of common coupling before the fault current limiter will be close to a sine wave. For this reason, an extra inductor may be integrated in the fault current limiter, or protective measures are taken in the controller so that the FCLID does not respond (fuse operation) when the fault is very near to it as explained in Chapter 5.

Other feeders connected to the point of common coupling will be subjected to the voltage waveform shown in Figure (6.2). The fundamental r.m.s value of this waveform is close to r.m.s value of the nominal voltage as explained in Chapter 2 (section 2.7). Also, the voltage will be more distorted for a fault closer to the fault current limiter. Additionally,

the harmonic current must be absorbed by the supply system. It is therefore advisable to improve the harmonic characteristics of the fault current limiter.

A method to reduce the harmonic content in the current during the operation of the fault current limiter is to modify the switching strategy. Instead of turning on the switches when the current reduces to 0 A, the semiconductor devices can be turned on at a higher current level. Figure (6.3) shows the simulated current waveform with Imin = 50 A. Its spectrum is shown in Figure (6.4).

It is observed that the effect of increasing Imin is to reduce the bandwidth of the limited fault current. This will increase switching frequency. Therefore device switching loss and system fault level during the FCLID operation should be considered as explained in Chapter 2 (section 2.5).

It is clear from the harmonic spectrum in Figure (6.4) that the harmonic current at the 3^{rd}, 5^{th}, 7^{th} still high. For such reason another switching strategy using a hysteresis current control has been proposed, the current waveform and its spectrum being shown in Figures 6.5 and 6.6. It can be noticed from the spectrum that the lower order harmonics have been improved with small increase in the higher harmonics. In this study the controller is designed for fixed Imin.

The harmonics in the FCLID current are of higher frequency and can be more easily absorbed using a passive filter at the point of common coupling. This also will improve the voltage at the PCC.

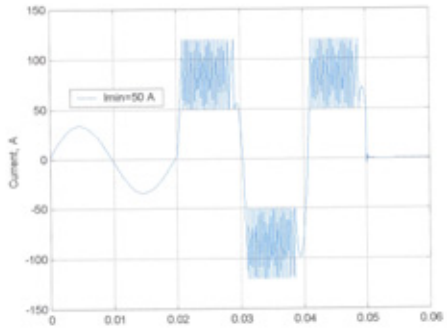


Figure 6.3 FCLID current with Imin=50A

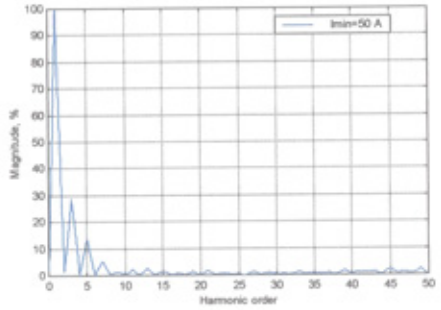


Figure 6.4 Frequency spectrum of the FCLID current with Imin=50A

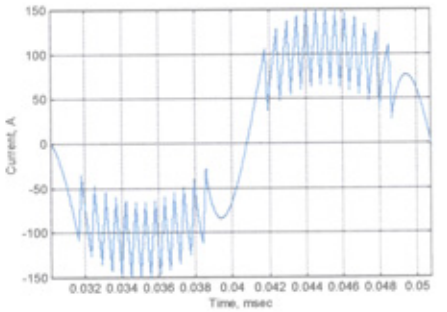


Figure 6.5 FCLID current with hysteresis current control

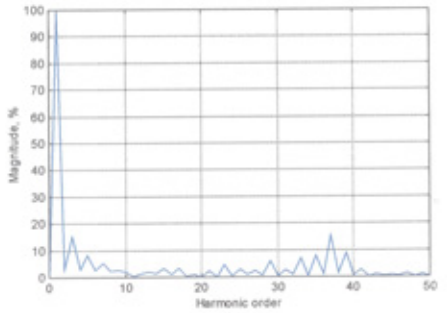


Figure 6.6 Frequency spectrum of the FCLID with hysteresis current control

6.3 Standards Regarding Short Duration Harmonics

Two main recognised standards dealing with harmonics have been considered:

IEEE Standard 519-1992, which states that for short duration harmonics "Devices such as a thyristor-controlled drive applied to a rolling mill generate short duration harmonic currents as the material passes through the mill. Generation of intermittent harmonics and the resulting voltage stress on the capacitors, the transformers, and other apparatus is sometimes more tolerable than the stress caused by the constant generation of harmonics." [83].

Engineering Recommendation G5/3 states that "Devices such as thyristor-controlled rolling mill drives may produce short-duration bursts of currents as a sheet or billet passes through the roller. Such short duration transients and harmonics are tolerable provided the current bursts and related voltage distortions are of an intermittent nature, e.g. the burst duration does not exceed 2 seconds and the interval between bursts is not less than 30 seconds. The principal concern is to prevent damage to other plant such as capacitors. Provided that the fundamental voltage at the metering point does not exceed the nominal supply voltage plus 6 per cent, there should be no risk of damage." [84].

The Engineering Recommendation G5/3 is updated to **Engineering Recommendation G5/4,** which states for "the load producing frequent bursts of harmonic (less than 3 s). Provided that the voltage change characteristics comply with the voltage change and flicker limit in Engineering Recommendation P28, it is unlikely that the additional contribution from such bursts of harmonic distortion need to be considered at the time of connection" [85].

Notching: "Equipment that results in voltage notching can only be connected if the level of distortion present at the PCC on the supply system is less than the appropriate planning level" [85].

Operation of the fault current limiter is a rare event as compared to a rolling mill drive, its duration is usually less than 2 seconds and the fundamental voltage at the PCC does not exceed the rated nominal voltage.

Also voltage notching may occur during the FCLID operation, when fault close to the FCLID. The depth of these notches can be reduced by connecting a small series inductor or by blocking the FCLID operation when the fault close to the PCC and let the fuse operate as explained in Chapter 5 (section 5.8).

According to the above standards, the harmonics produced by the fault current limiter may not be a problem. This is particularly the case if the harmonics are reduced using the modulation control. Nevertheless, the risk of damage to the FCLID and other equipment must be prevented. Therefore, the possibility of harmonic resonance with the supply network and loads connected to the point of common coupling has been investigated and is presented in the following section.

6.4 Consideration of Harmonic Resonance

It has been shown that during the operation of the FCLID, harmonics over a quite wide spectrum band are produced. The worse case is that some harmonics could coincide with the natural frequencies of the circuit formed by power factor correction capacitor at the point of common coupling and the supply system impedance in the upstream. If this happens, the harmonics injected into the supply system will be amplified and over voltage/current may cause damage to the plant. To analyse the situation, harmonic current

flow analysis for the distribution network shown in Figure (2.4) has been carried out. A simple equivalent circuit of the network is shown in Figure (6.7), where the FCLID is assumed to be a source of harmonic current *In*. The current at any harmonic frequency divides between the shunt capacitor and supply as:

$$In = Icn + Isn \tag{6.1}$$

where *In* is the harmonic current generated; *Isn* is the harmonic current that flows into the supply system; *Icn* is the harmonic current that flows into the capacitor.

Then,

$$Isn = \frac{Zc}{Zs + Zc} \times In \tag{6.2}$$

$$Icn = \frac{Zs}{Zs + Zc} \times In \tag{6.3}$$

where Zs and Zc are the impedances of the supply system and capacitor, respectively at the frequency examined.

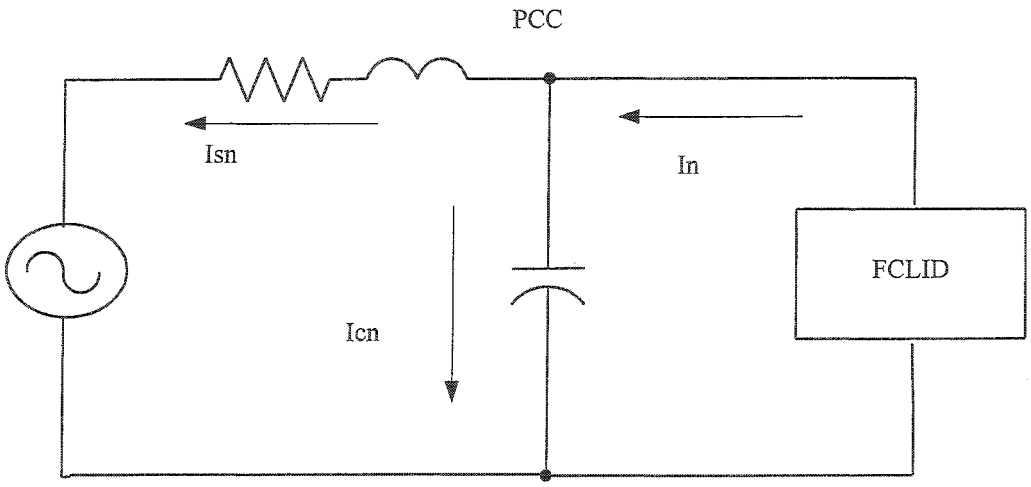


Figure 6.7 Harmonic current flow

Harmonic resonance corresponds to the case when the inductive reactance of the supply equals the capacitive reactance of the capacitor. Both *Isn* and *Icn* will be greater than *In*. Analysis is performed for different values of the capacitance and system fault level. The ratio *Isn/In* is plotted in Figure (6.8) for a system fault level of 1 kA. The shunt capacitance is varied from 1 mF to 10 mF and the resonant peak is captured for each capacitance value. It is clear that the switching frequency should avoid the range from 200 Hz to 800 Hz. If the switching frequency of the FCLID is increased above 800 Hz by setting proper Imax and Imin, there should be no risk of parallel resonance.

It is worth pointing out that this is the worse case where power factor correction capacitors are connected directly at the PCC shown in Figure (2.4). A small series inductor will be useful to limit the current spikes in the capacitor and to protect the IGBT from high di/dt due to the discharging of the capacitor during turn-on.

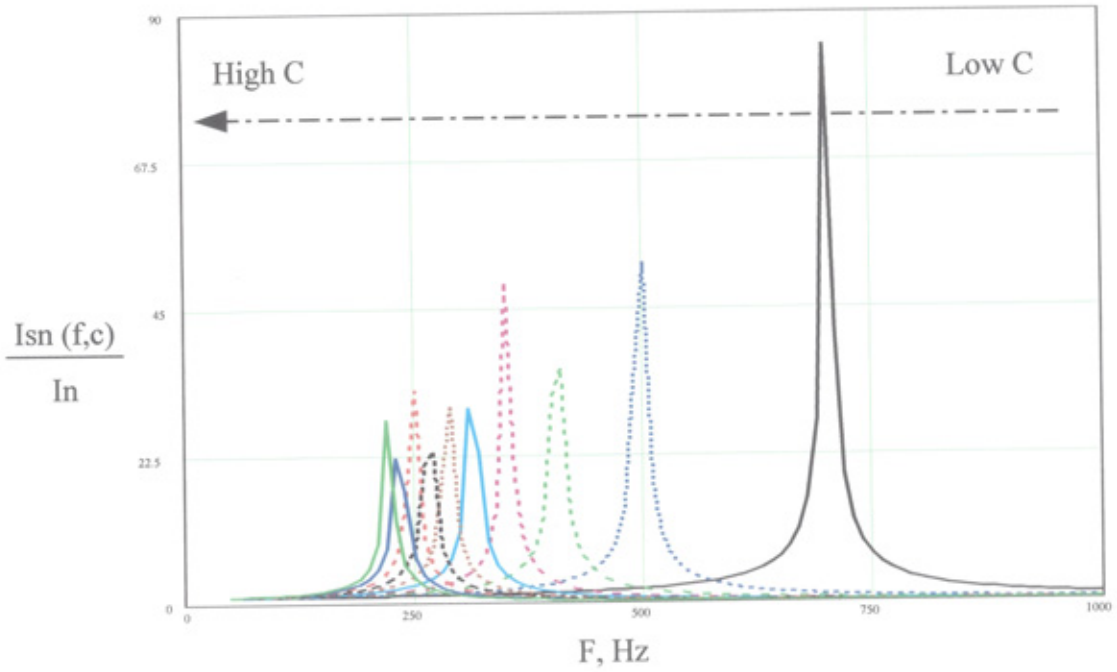


Figure 6.8 Resonant peak with different capacitance values

The need for an inductor and its rating depends on the application and the location of the FCLID with respect to the PCC. If the fault occurs close to the FCLID (zero impedance), the fuse will operate before the FCLID start switching. In this case, there is no need for the inductor.

The cable capacitance and inductance could also introduce a resonant mode. For the 230 V single-phase circuit, the cable capacitance is about 1 μF per km and inductance is about 230 μH per km. The natural frequency at which parallel resonance occurs may be estimated as:

$$f_o = \frac{1}{2 \times \pi \times l} \sqrt{\frac{1}{L \times C}} \tag{6.5}$$

Where f_o is the resonance frequency and l is the cable length in kilometres.

Figure (6.9) shows the relationship between the resonance frequency and cable length. The supply fault current level is assumed to be 1 kA. It is clear that for cables shorter than 5 km, which is usually the case for low voltage radial distribution network, there is no risk of resonance as long as the switching frequency of the FCLID is under 2 kHz. Too high a switching frequency should also be avoided to prevent excessive switching losses in the solid-state device and varistor.

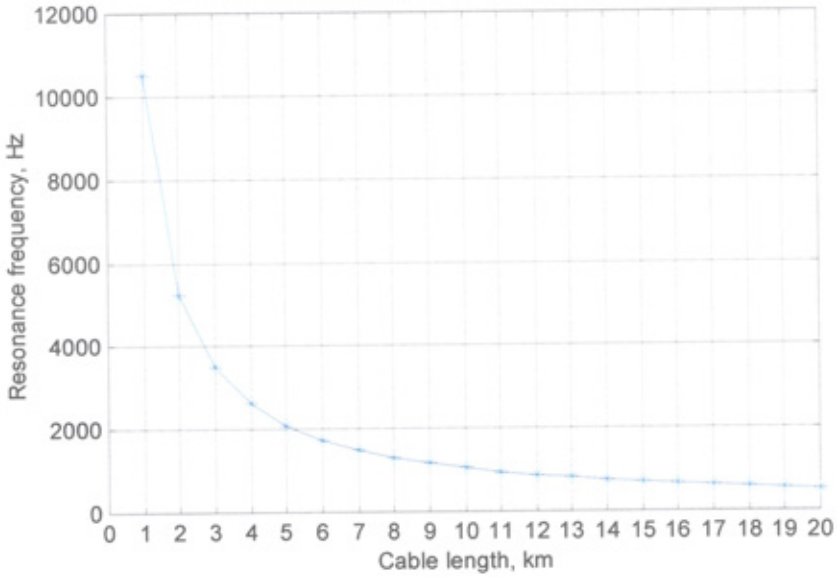


Figure 6.9 Resonance frequency versus cable length

6.5 Experimental Results

An experiment set-up was built to represent the network shown in Figure (5.23). The line current and voltage as well as the current in other load connected at the point of common coupling were recorded. Figures 6.10 and 6.11 show a cycle of the line current and its frequency spectrum with Imax = 120 A and Imin = 0 A. Figures 6.12 and 6.13 present the same waveform but with Imin = 50 A. Good agreement is observed between the experimental results (Figures 6.11 and 6.13) with the simulation results from section 6.2 (Figures 6.1 and 6.4). Previous analysis and conclusions made based on computer simulation studies are therefore validated.

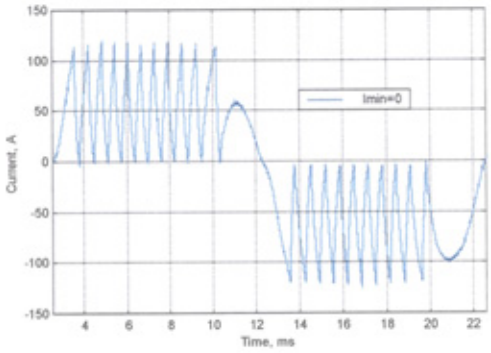


Figure 6.10 Measured FCLID current waveform (I_{fault} =1 kA)

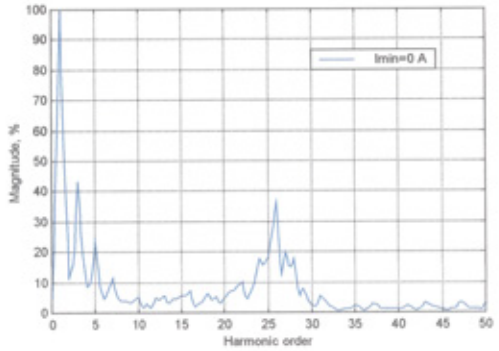


Figure 6.11 Frequency spectrum of measured FCLID current

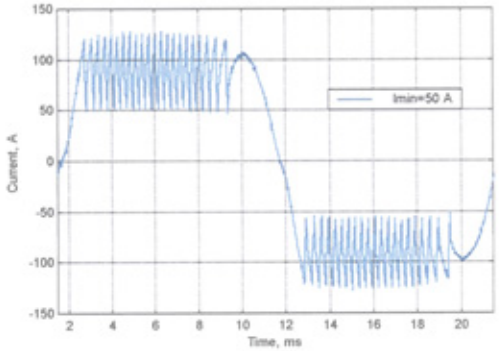


Figure 6.12 Measured FCLID current waveform (I_{fault} =1 kA)

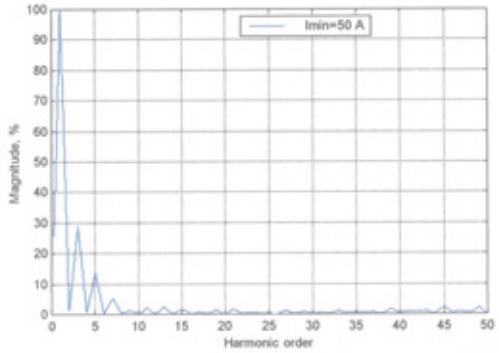


Figure 6.13 Frequency spectrum of measured FCLID current

6.6 Effect of The FCLID on The Switched Mode Power Supply (SMPS)

Typical loads that are sensitive to the distorted waveforms produced by the FCLID are domestic and commercial electronic equipment such as a PC (personal computer) and TV (television) [86]. Such equipment normally includes switch mode power supply (SMPS). As shown in Figure (6.14), the SMPS derives its power from the utility supply via a diode rectifier with a capacitively smoothed DC link. The input current is usually discontinuous as shown in Figure (6.15) [87]. It is useful to consider the effects of the proposed FCLID on such load when connected to the point of common coupling in the distribution network.

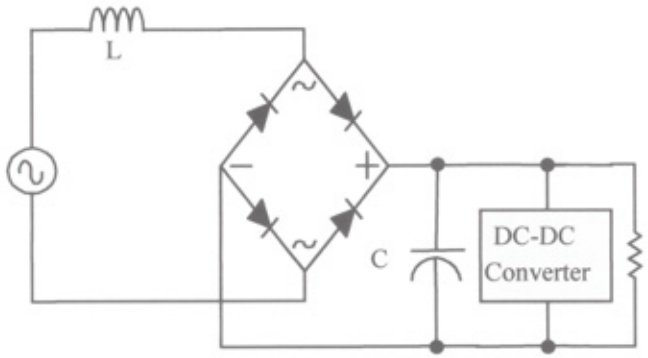


Figure 6.14 Switch mode power supply

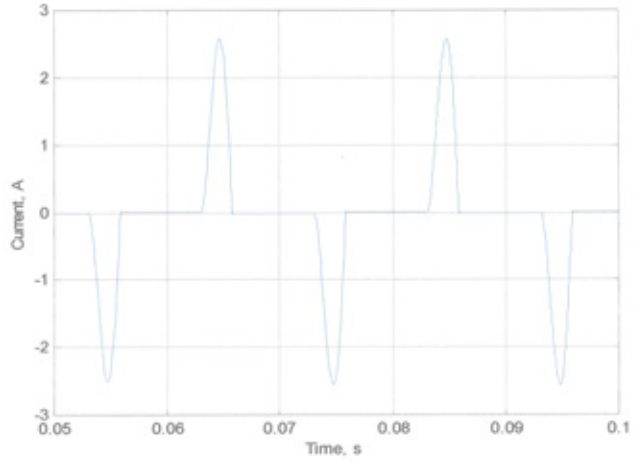


Figure 6.15 Input current to SMPS

A main concern is that the FCLID may affect the operation of the SMPS due to the high rate of change of voltage when the semiconductor device in the FCLID is turned off and the clamping voltage of the varistor appears across the FCLID. Two tests have been performed: case 1, when short-circuit fault is far from the FCLID as shown in Figure (6.16) and case 2 for fault close to the FCLID as shown in Figure (6.17). In both cases the prospective fault current is 1 kA. A PC is connected in front of the FCLID. Figures 6.18 and 6.19 show the PC current and voltage waveforms for case 1 and the corresponding wave-forms for case 2 are shown in Figures 6.20 and 6.21.

It is shown that the high dv/dt applied at the input of the SMPS will be seen by the d.c. link capacitor, causing input current spikes. The spikes are higher when the fault is close to the fault current limiter and hence the PCC. The current spikes may exceed the fuse rating of the SMPS and cause fuse fatigue. Figure (6.24) shows the moment when the PC fuse blew at 220 ms after the fault current limiter started operating.

The second problem, which may rise, particularly when the fault is close to the FCLID, is that more zero crossing points are introduced in the voltage waveform. This may affect the operation of equipment that is phase-locked to the sinusoidal supply voltage.

A simulation model is used to recreate the situation shown in Figures 6.20 and 6.21. The results are given in Figures 6.22 and 6.23. Similar signatures can be observed between the simulation and experiment if the measured waveforms are zoomed in. As a solution to the above problem, a small inductor of 100 μH may be inserted in series with the FCLID. During the normal operation the FCLID is bypassed by a vacuum circuit-breaker,

therefore insertion of the series inductor will not cause problems (losses, voltage drop or overvoltage). The simulation results for this case are shown in Figures 6.24 and 6.25.

The size of the inductor depends on the short-circuit level, limited fault current and location of the FCLID from the point of common coupling. Also the needs for the inductor depends on the application as explained in Section 6.4.

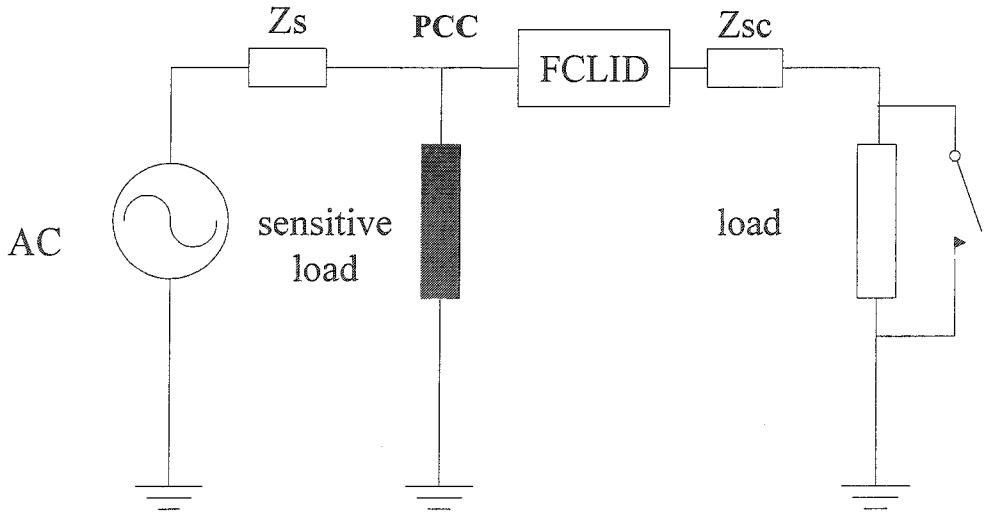


Figure 6.16 Test circuit for faults far from the FCLID

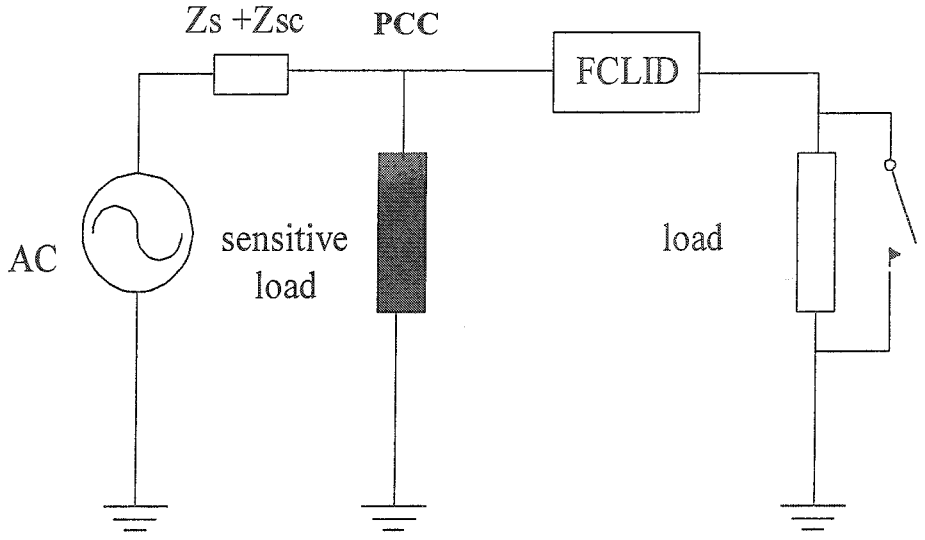


Figure 6.17 Test circuit for faults close to the FCLID

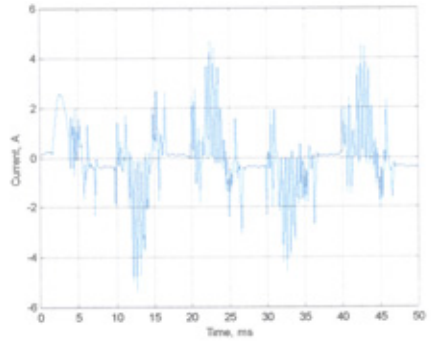


Figure 6.18 PC current for a remote fault

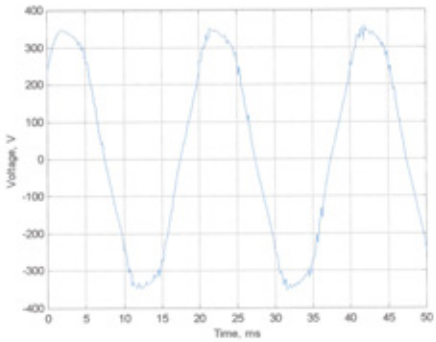


Figure 6.19 PC Voltage with a remote fault

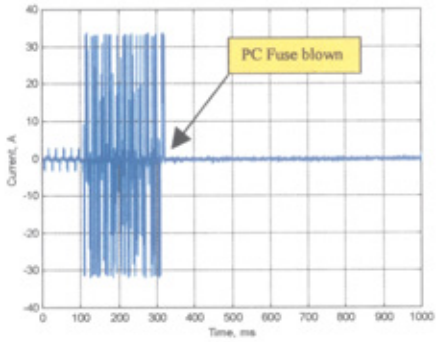


Figure 6.20 PC current for a fault close to the FCLID

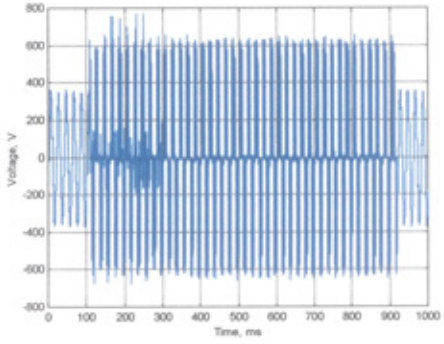


Figure 6.21 PC voltage for a fault close to the FCLID

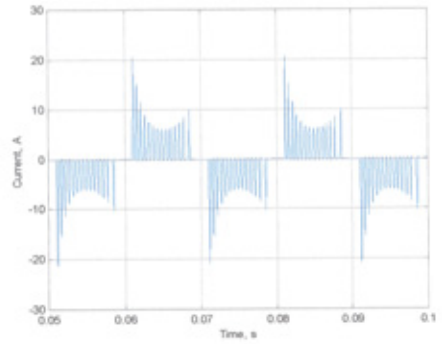


Figure 6.22 Simulated PC current

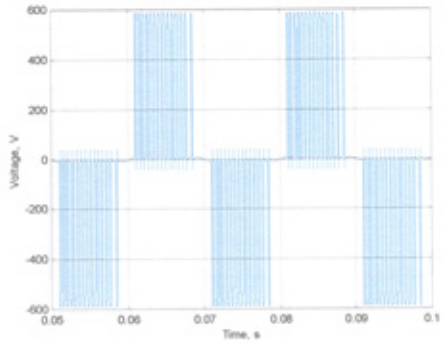


Figure 6.23 Simulated PC voltage

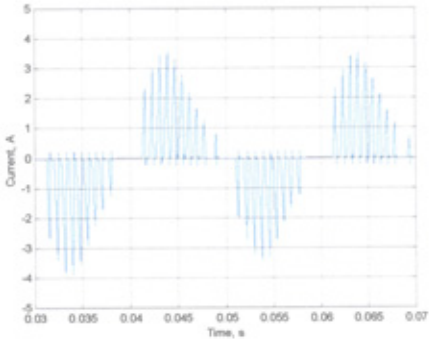


Figure 6.24 PC current with series inductor

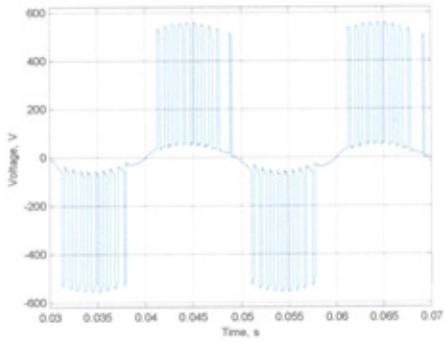


Figure 6.25 PC voltage with series inductor

6.7 Conclusions

In this chapter, the problems associated with harmonics generation in the proposed FCLID have been analyzed. Simulation and experimental tests are performed regarding the application of the FCLID in a typical 230 V single-phase distribution network. Factors affecting the harmonic characteristics are identified. The risk of harmonic resonance and adverse effects on sensitive loads such as SMPS are assessed and remedy actions are recommended. The results obtained from simulation and the experimental test show that:

- Operation of the proposed FCLID will produce high level of harmonic currents, which need to be reduced by controlling Imax and Imin, taking into account the effect of increasing Imin on the varistor and solid-state device.
- The operation of the FCLID should not exceed 2 seconds in order for the short duration harmonics produced by the FCLID comply with the harmonics standards (IEEE 519-1992 and G5/3).
- Proper measures should be taken to avoid the risk of harmonic resonance between the cable or power factor correction capacitors, and the supply network inductance. Insertion of a small series inductor might be necessary in certain applications, to attenuate the undesirable effects on sensitive loads such as SMPS. The voltage waveform at the point of common coupling is also improved. The size of the inductor depends on location of the FCLID with respect to the PCC, short-circuit level and application.

CHAPTER SEVEN

CONCLUSIONS

In this thesis a new device capable of limiting and interrupting fault currents in power distribution networks has been designed, built and tested. The Fault Current Limiting and Interrupting Device (FCLID) studied combines the advantages of both the FCLD and the FCID. In addition, it is suitable for transformer and feeder protection where co-ordination with conventional downstream protection devices is required.

The main contributions of the work presented can be summarised as follows:

First, a criterion to determine the stress on the IGBT and varistor for this type of application has been developed.

Next, an alternative technique using an infrared thermal imaging system for measuring the energy handling capability of ZnO varistors under continuous repetitive pulses has been proposed. The advantage of this method is that, unlike thermocouples, it can measure the varistor surface temperature not only at a single point. Furthermore, it has a faster response than the thermocouple so that the measurement under transient conditions (repetitive pulses) is possible.

Then, a method that allows improved current sharing between parallel varistors (by connecting a small series resistor with each varistor) has been developed. Such a resistor does not change the clamping voltage; overall V-I characteristics being only slightly affected. The advantages of this technique over the existing one reported in the literature

are easier implementation, reduced testing time for matching the varistor characteristics and lower cost.

In addition, a method for predicting the junction temperature of a solid-state switch under transient condition has been developed. The advantages of this method over the old techniques (which were suitable for steady-state operation only) is that it is able to predict the junction temperature of the solid-state switch in advance (up to 1 s). This allows enough time for the controller to appropriately adjust its parameters and prevent damage of the IGBT. Also, the experimental tests for obtaining the device characteristics (collector-emitter voltage and switching power losses) is no longer needed.

A method for predicting the varistor temperature under repetitive pulses has also been developed. The relationship between the input energy to the varistor and temperature is linear during normal region, so the varistor temperature can be predicted by measuring the energy input. This method is superior than the existing ones (such as thermocouple or infrared camera) since it has faster response and it is less costly.

Finally, an experimental test system for a single-phase 230 V FCLID prototype has been developed and evaluated.

In order to verify the above statements a computer model of the FCLID was designed using MATLAB/Simulink and Power System Blockset. This model was implemented into a typical power distribution network and its performance was analysed. Simulation studies have shown that the FCLID can effectively handle all types of faults in a three-phase system. For a line to line fault, the losses of the device are less than in the other cases (single line-to-ground or double line-to-ground faults). Also it is possible to switch

off one phase and let the other phase supply the load (assuming that the total current is within the specified rating). It has also been demonstrated that the FCLID improves the quality of supply by mitigating the voltage sags during system faults and by preventing unnecessary fuse operation. In addition, it can reduce the phase angle jump thus preserving the system stability.

Due to the switching action of the IGBT during the FCLID operation, its junction temperature may exceed the maximum allowable value. Therefore, a new method is proposed to predict the IGBT junction temperature. It is based on measurement of voltage across and current through the IGBT and information about the transient thermal impedance of the device. Thus, the performance of this method directly depends on the accuracy of the measuring instrument and the transient thermal impedance model. By implementing this method, the FCLID can be operated under different conditions, as long as its junction temperature is within the normal operating range.

The analysis of the varistor performance has shown that the infrared imaging system is a useful mean for measuring the energy handling capability, temperature distribution and uniformity of the microstructure of the varistor. Commercially available varistors can be used for repetitive pulses applications with energy handling capability equal to twice its rating per pulse as specified in the manufacturer data sheet. The tests carried out on the varistors have shown that there exist three operating regions when a varistor is subjected to continuous repetitive pluses: thermal stability region, the out of thermal stability region and thermal runaway region.

The FCLID produces undesirable harmonics that are injected into the supply grid. The harmonic spectra can be improved by controlling the device parameters, mainly Imax and Imin. It has also been demonstrated that the harmonic currents produced by the FCLID do not exceed the standardised levels specified in IEEE 519-1992, G5/3 and G5/4.

Suggestions for Further Work

- The research work described in this thesis has resulted in the development of a 30 kVA FCLID suitable for 230/400 V distribution networks. To obtain the full potential of the FCLID in high power applications, further work is required to develop a smart controller which is able to predict the temperatures of the solid-state device and varistor, estimate the short-circuit level and accordingly define the operating mode of the FCLID based on the estimated system conditions.
- The results obtained from the three-phase system analysis show that the FCLID is capable to work for all types of three-phase faults. Further work is required to verify these results experimentally using a three-phase FCLID.
- This research used a new method for improving current sharing between parallel varistor to achieve the FCLID rating. Implementing a high power FCLIDs needs further investigations to find a cooling system to increase the energy handling capability of varistors.
- The proposed technique for temperature prediction of IGBTs can be used for other applications such as drive system, a.c. and d.c. power converters. Further work is required to make this method suitable for both transient and normal conditions of semiconductor devices.

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APPENDIX A

A CRITERION FOR CALCULATING THE STRESS ON THE IGBT AND VARISTOR

A.1 Calculation of Switching Frequency during FCLID Operation

To investigate the performance of the FCLID under different short-circuit current level, the switching frequency will be calculated. A typical distribution network under short circuit conditions may be represented by its Thevenen equivalent circuit as shown in Figure (A.1). This circuit represents the network when the FCLID switching device is ON and a short-circuit occurs. That is the rising edge of the fault current as shown in Figure (A.2).

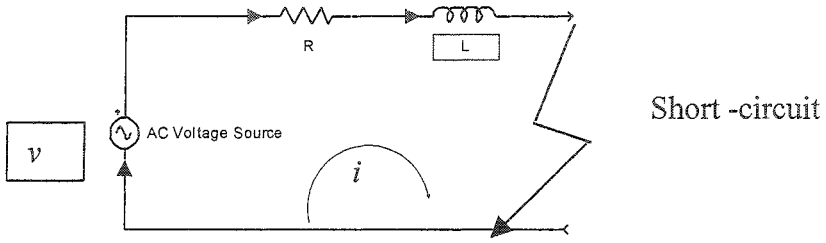


Figure A.1

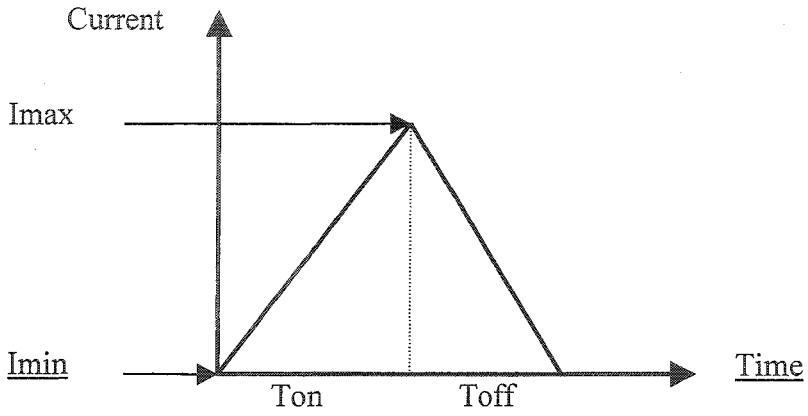


Figure A.2

$$v = iR + L\frac{di}{dt} \tag{A.1}$$

Assuming that the supply voltage is constant. The solution of equation (A.1) gives the short-circuit current (during rising edge)

$$v = iR + L\frac{di}{dt} \tag{A.2}$$

Where R is the resistance of (supply + IGBT + diode + cable) and L is the inductance of the (supply + cable).

Taking Laplace transform for both side of equation (A.2)

$$\frac{v}{s} = I_{(s)}R + L(sI_{(s)} - I_o) \tag{A.3}$$

By taking inverse Laplace for the both side the current equation can be expressed as

$$i = \frac{v}{R}(1 - e^{-\frac{t}{\tau}}) + I_o e^{-\frac{t}{\tau}} \tag{A.4}$$

I_o = Imin

At t = Ton, I = Imax

Substituting in equation (A.4).

$$\mathrm{Im}ax = \frac{v}{R}(1 - e^{-\frac{Ton}{\tau}}) + \mathrm{Im}in\, e^{-\frac{Ton}{\tau}} \tag{A.5}$$

$$e^{-\frac{Ton}{\tau}} = \frac{(v/R - \mathrm{Imax})}{(v/R - \mathrm{Imin})} \tag{A.6}$$

The value of Ton can be obtained by taking the logarithm for both side of equation (A.6).

$$Ton = \frac{-L}{R} \times ln\, \frac{(v/R - \mathrm{Imax})}{(v/R - \mathrm{Imin})} \tag{A.7}$$

Because the supply voltage is sinusoidal so the pulse width is varying.

$v = \sqrt{2} \times V_{rms} \times \sin \omega t$, Where ωt is the instant of the switching.

In order to get Ton at any instant, substituting the value of v in equation (A.7), so Ton can be written as

$$Ton = \frac{-L}{R} \times ln\, \frac{(\sqrt{2} \times V_{rms} \times \sin \omega t / R - \mathrm{Imax})}{(\sqrt{2} \times V_{rms} \times \sin \omega t / R - \mathrm{Imin})} \tag{A.8}$$

when the switching device is turned off the circuit may be represented as shown Figure (A.3).

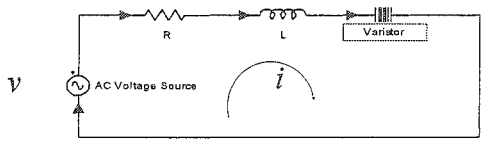


Figure A.3

Assuming that the varistor clamping voltage is constant and equal to the calmping voltage (V_c) at I = Imax

$$v = i R_1 + L \frac{di}{dt} + V_c \tag{A.9}$$

Where R_1 is the resistance of (supply + cable) and L is the inductance of the (supply + cable).

Taking Laplace transform for both side of equation (A.9)

$$\frac{v - V_c}{s} = I_{(s)} R_1 + L(sI_{(s)} - I_o) \tag{A.10}$$

By taking inverse Laplace for the both side the current equation will be:

$$i = \frac{v - V_c}{R_1}(1 - e^{-\frac{t}{\tau}}) + I_o e^{-\frac{t}{\tau}} \tag{A.11}$$

I_o = Imax

At $t = T_{off}$ $I = Imin$

Substituting in equation (A.11).

$$\mathrm{Im}\,in = \frac{v - V_c}{R_1}(1 - e^{-\frac{Toff}{\tau}}) + \mathrm{Im}\,ax\, e^{-\frac{Toff}{\tau}} \tag{A.12}$$

$$e^{-\frac{Toff}{\tau}} = \frac{(v - V_c / R_1 - \mathrm{Imin})}{(v - V_c / R_1 - \mathrm{Imax})} \tag{A.13}$$

The T_{off} time can be determined by taking the logarithm for both side of equation (A.13)

$$T_{off} = \frac{-L}{R_1} \times ln \frac{((v - V_c) / R_1 - \mathrm{I\,min})}{((v - V_c) / R_1 - \mathrm{I\,max})} \tag{A.14}$$

$$T_{off} = \frac{-L}{R_1} \times ln \frac{((\sqrt{2} \times V_{rms} \times \sin(\omega t + T_{on}) - V_c) / R_1 - \mathrm{I\,min})}{((\sqrt{2} \times V_{rms} \times \sin(\omega t + T_{on}) - V_c) / R_1 - \mathrm{I\,max})} \tag{A.15}$$

Equations 16 give the pulse width (T_p) at one switching angle.

$$T_p = T_{on} + T_{off} \tag{A.16}$$

The average pulse width can be calculating as:

$$T_{pav} = \frac{\sum_{wt=10}^{90} -L}{g} \left[\frac{1}{R} \times ln \frac{(\sqrt{2} \times V_{\sim} \times \sin \omega t / R - \mathrm{Imax})}{(\sqrt{2} \times V_{\sim} \times \sin \omega t / R - \mathrm{Imin})} + \frac{1}{R_1} \times ln \frac{((\sqrt{2} \times V_{\sim} \times \sin(\omega t + Ton) - V_c) / R_1 - \mathrm{I\,min})}{((\sqrt{2} \times V_{\sim} \times \sin \omega t + Ton - V_c) / R_1 - \mathrm{I\,max})} \right] \tag{A.17}$$

Where g is the number of times of calculating Tp. So the number of pulses (N) per each half cycle is given by equation (A.18)

$$N = \frac{10 \times 10^{-3}}{T_{pav}} \tag{A.18}$$

The switching frequency (F) for each IGBT during the FCLID operation can be obtained from equation (A.19)

$$F = N \times 50 \tag{A.19}$$

A.2 Calculation of the Energy Absorbed by the Varistor During FCLID Operation

Based on the calculation of the switching frequency, so the energy absorbed by the varistor during the FCLID operation can be obtained from equation (A.20).

$$E = V_c \times I_{max} \times . T_{off(av)} \times N \tag{A.20}$$

Where,

E is the energy absorbed by the varistor for one cycle.

V_c is the varistor clamping voltage at I = Imax (from data sheet).

$T_{off(av)}$ is the average turn off time.

N is the number of pulses per each half cycle.

In case of Imin > 0 the fault current transferred to the IGBT at i= Imin, and the current flowing through the varistor will decay until it reach zero (assuming the current will decay at fixed slop), so the energy equation can be expressed as:

$$E = V_c \times I_{max} \times . T_{off\,(av)} \times N \times (1 + \frac{Imin}{Imax}) \qquad (A.21)$$

A MATHCAD program was developed to calculate the switching frequency and input energy to the varistor at different conditions (different short-circuit levels and different Imin). Both the mathematical and simulation results are in good agreement as shown in Figures 2.8-2.11.

APPENDIX B

VARISTOR TERMIOLOGY

Definitions (IEEE Standard C62.33, 1982)

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, or thermal, and can be expressed as a value for stated conditions. A rating is a value which establishes either a limiting capability or a limiting condition (either maximum or minimum) for operation of a device. It is determined for specified values of environment and operation. The ratings indicate a level of stress which may be applied to the device without causing degradation or failure. Varistor symbols are defined on the linear V-I graph illustrated in Figure (B.1) and Table B.1 defines the terminology used in varistor specifications.

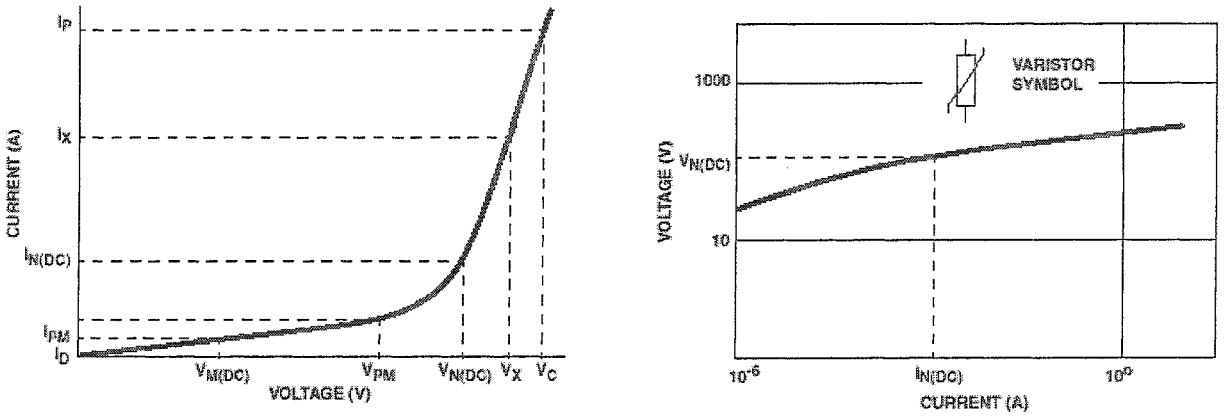


Figure B.1

SYMBOL	TERMS AND DESCRIPTIONS
$V_{N(DC)}$	**Nominal Varistor Voltage.** Voltage across the varistor measured at specified pulsed current, $I_{N(DC)}$, of specific duration. The value of $I_{N(DC)}$ is defined by the manufacturer.
V_c	**Clamping voltage.** Peak voltage across varistor measured under conditions of specified peak V_C pulse current and specified wave form. **Note:** peak voltage and peak current are not necessarily coincidental in time
V_x	Voltage across the varistor measured at a given current
α	**Non-linear Exponent.** A measure of varistor nonlinearity between two given operating currents, I1 and I2, as described by $I = kV^{\alpha}$ where k is the device constant, $I_1 \leq I \geq I_2$, and $\alpha_{12} = \frac{\log I_2 / I_1}{\log V_2 / V_1}$
Rx	**Resistance (Varistor).** Static resistance of the varistor at a given operating point as defined by: $R_x = \frac{V_x}{I_x}$
Z_x	**Dynamic Impedance (Varistor).** A measure of small signal impedance at a given operating point as defined by: $Z_x = \frac{dV_x}{dI_x}$
W_{TM}	**Rated Single Pulse Transient Energy (Varistor).** Energy which may be dissipated for a single impulse of maximum rated current at specified waveshape, with rated RMS voltage or DC voltage also applied, without causing device failure.
$P_{T(AV)M}$	**Rated Transient Average Power Dissipation (Varistor).** Maximum average power which may be dissipated due to group of pulses occurring within specified isolated time period, without causing device failure

Table B.1 Varistor symbols and definitions

APPENDIX C

CIRCUIT DIAGRAM OF THE FCLID CONTROLLER

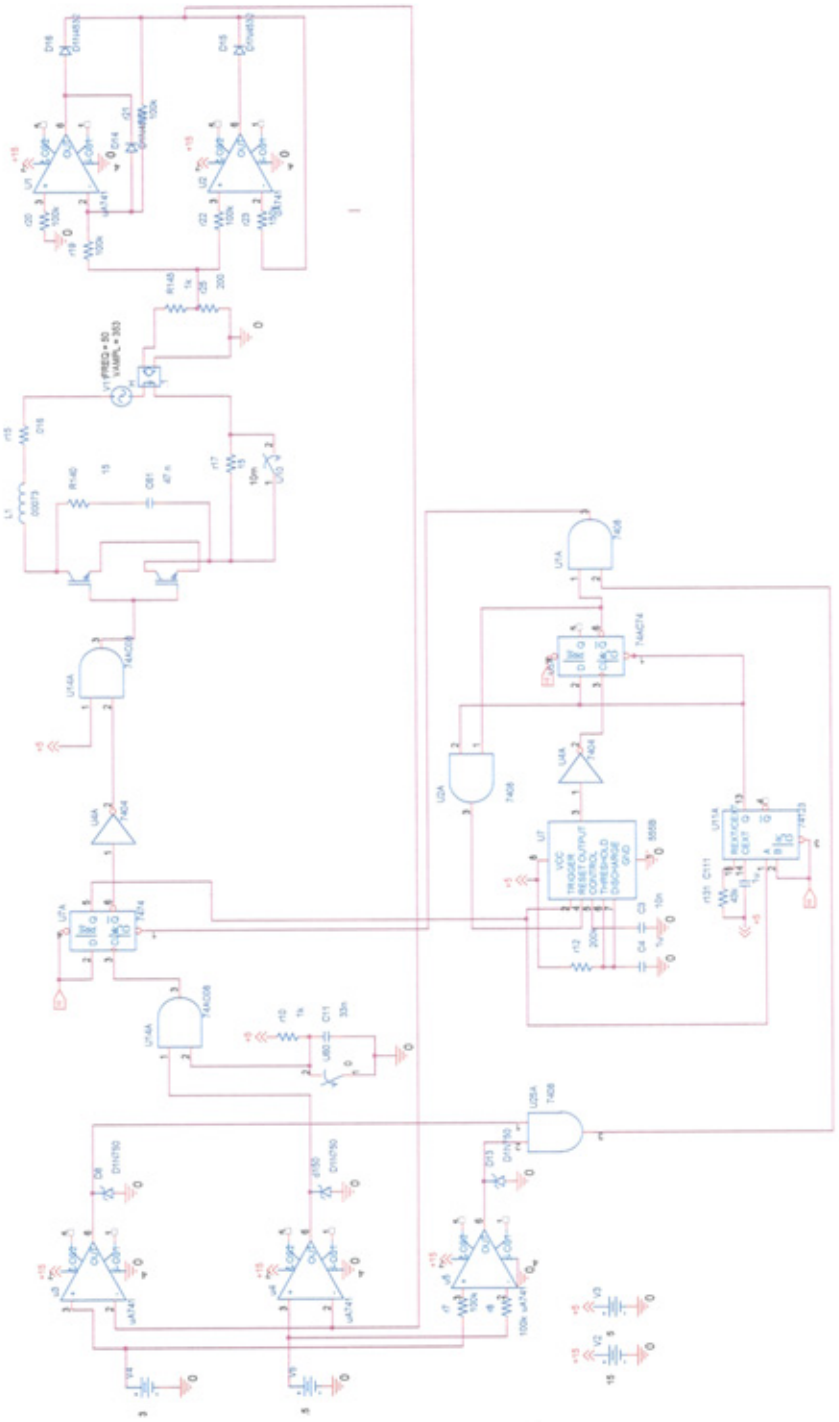


Figure C.1 Circuit diagram of the FCLID controller

APPENDIX D

IGBT DATA SHEET

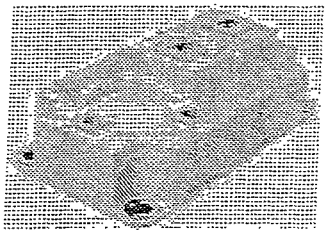
SEMIKRON

Absolute Maximum Ratings Symbol	Conditions [1]	Values	Units
V_{CES}		1200	V
V_{CGR}	R_{GE} = 20 kΩ	1200	V
I_C	T_{case} = 25/80 °C	300 / 220	A
I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	600 / 440	A
V_{GES}		± 20	V
P_{tot}	per IGBT, T_{case} = 25 °C	1660	W
T_j, (T_{stg})		– 40 . . . +150 (125)	°C
V_{isol}	AC, 1 min.	2 500 [7]	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	40/125/56	
Inverse Diode			
I_F = – I_C	T_{case} = 25/80 °C	300 / 200	A
I_{FM} = – I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	600 / 440	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	2200	A
I^2t	t_p = 10 ms; T_j = 150 °C	24200	A^2s

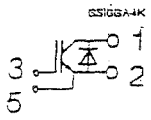
Characteristics Symbol	Conditions [1]	min.	typ.	max.	Units
$V_{(BR)CES}$	V_{GE} = 0, I_C = 3 mA	≥ V_{CES}	–	–	V
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 8 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, T_j = 25 °C	–	0,4	4	mA
	V_{CE} = V_{CES}, T_j = 125 °C	–	18	–	mA
I_{GES}	V_{GE} = 20 V, V_{CE} = 0	–	–	1	µA
V_{CEsat}	I_C = 200 A, V_{GE} = 15 V;	–	2,5(3,1)	3(3,7)	V
V_{CEsat}	I_C = 300 A, T_j = 25 (125) °C	–	3,0(3,8)	–	V
g_{fs}	V_{CE} = 20 V, I_C = 200 A	110	–	–	S
C_{CHC}		–	1300	1500	pF
C_{ies}	V_{GE} = 0	–	15	19	nF
C_{oes}	V_{CE} = 25 V	–	2	2,6	nF
C_{res}	f = 1 MHz	–	1,0	1,3	nF
L_{CE}		–	–	20	nH
$t_{d(on)}$	V_{CC} = 600 V	–	250	400	ns
t_r	V_{GE} = +15 V, -15V [3]	–	90	160	ns
$t_{d(off)}$	I_C = 200 A, ind. load	–	550	700	ns
t_f	R_{Gon} = R_{Goff} = 4,7 Ω	–	70	100	ns
E_{on} [5]	T_j = 125 °C	–	26	–	mWs
E_{off} [5]		–	22	–	mWs
inverse Diode [8]					
V_F = V_{EC}	I_F = 200 A, V_{GE} = 0 V;	–	2,0(1,8)	2,5	V
V_F = V_{EC}	I_F = 300 A, T_j = 25 (125) °C	–	2,25(2,1)	–	V
V_{TO}	T_j = 125 °C	–	–	1,2	V
r_T	T_j = 125 °C	–	3	5,5	mΩ
I_{RRM}	I_F = 200 A; T_j = 25 (125) °C [2]	–	80(120)	–	A
Q_{rr}	I_F = 200 A; T_j = 25 (125) °C [2]	–	11(29)	–	µC
Thermal Characteristics					
R_{thjc}	per IGBT	–	–	0,075	°C/W
R_{thjc}	per diode D	–	–	0,15	°C/W
R_{thch}	per module	–	–	0,038	°C/W

SEMITRANS® M
IGBT Modules

SKM 300 GA 123 D



SEMITRANS 4



GA

Features
- MOS input (voltage controlled)
- N channel, Homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 * I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes [8]
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (12 mm) and creepage distances (20 mm).

Typical Applications: → B 6-167
- Switching (not for linear use)

1) T_{case} = 25 °C, unless specified
2) I_F = – I_C, V_R = 600 V, – di_F/dt = 2000 A/µs, V_{GE} = 0 V
3) Use V_{GEoff} = -5 ... -15 V
5) See fig. 2 + 3; R_{Goff} = 4,7 Ω
7) V_{isol} = 4000 V_{rms} on request
8) CAL = Controlled Axial Lifetime Technology.

Cases and mech. data → B6-168
SEMITRANS 4

SEMIKRON

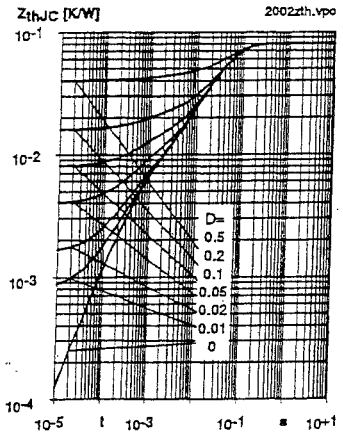


Fig. 19 Transient thermal impedance of IGBT
$Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

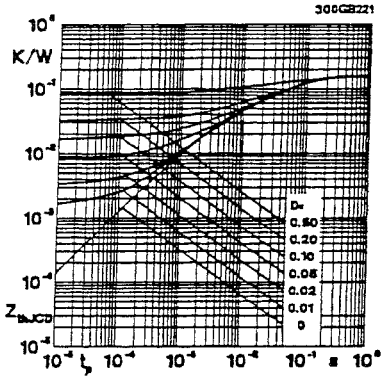


Fig. 20 Transient thermal impedance of inverse CAL diodes $Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

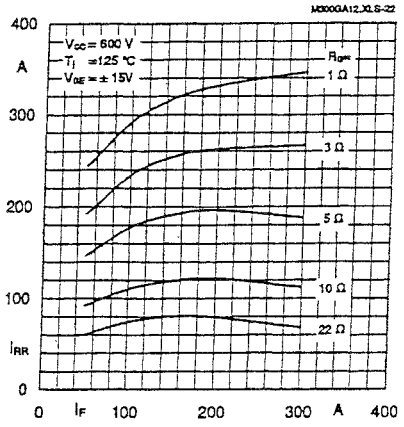


Fig. 22 Typ. CAL diode peak reverse recovery current $I_{RR} = f(I_R; R_G)$

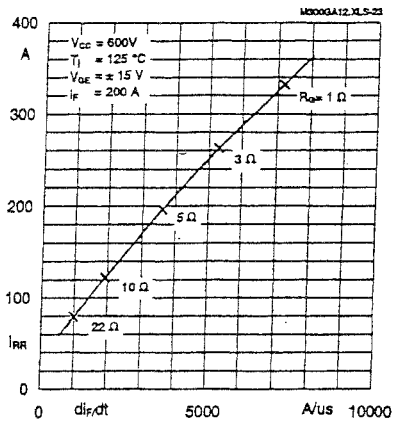


Fig. 23 Typ. CAL diode peak reverse recovery current $I_{RR} = f(di/dt)$

Typical Applications include

Switched mode power supplies
DC servo and robot drives
Inverters
DC choppers
AC motor speed control
Inductive heating
UPS Uninterruptable power supplies
General power switching applications
Electronic (also portable) welders
Pulse frequencies also above 15 kHz

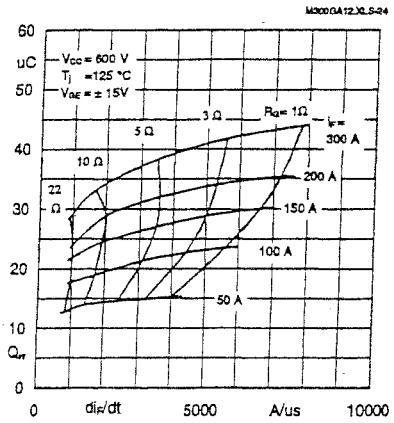


Fig. 24 Typ. CAL diode recovered charge